

# Rocket BSW 11.6" Schematic

## Braswell

**2015-11-09**  
**REV : A00**

*DY : None Installed*  
*OSP/ISP : different config for storage and DRAM*  
*Drax : stuff on Drax*

Rocket BSW 1st



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Title

**Cover Page**

Size  
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**Rocket BSW 11.6"**

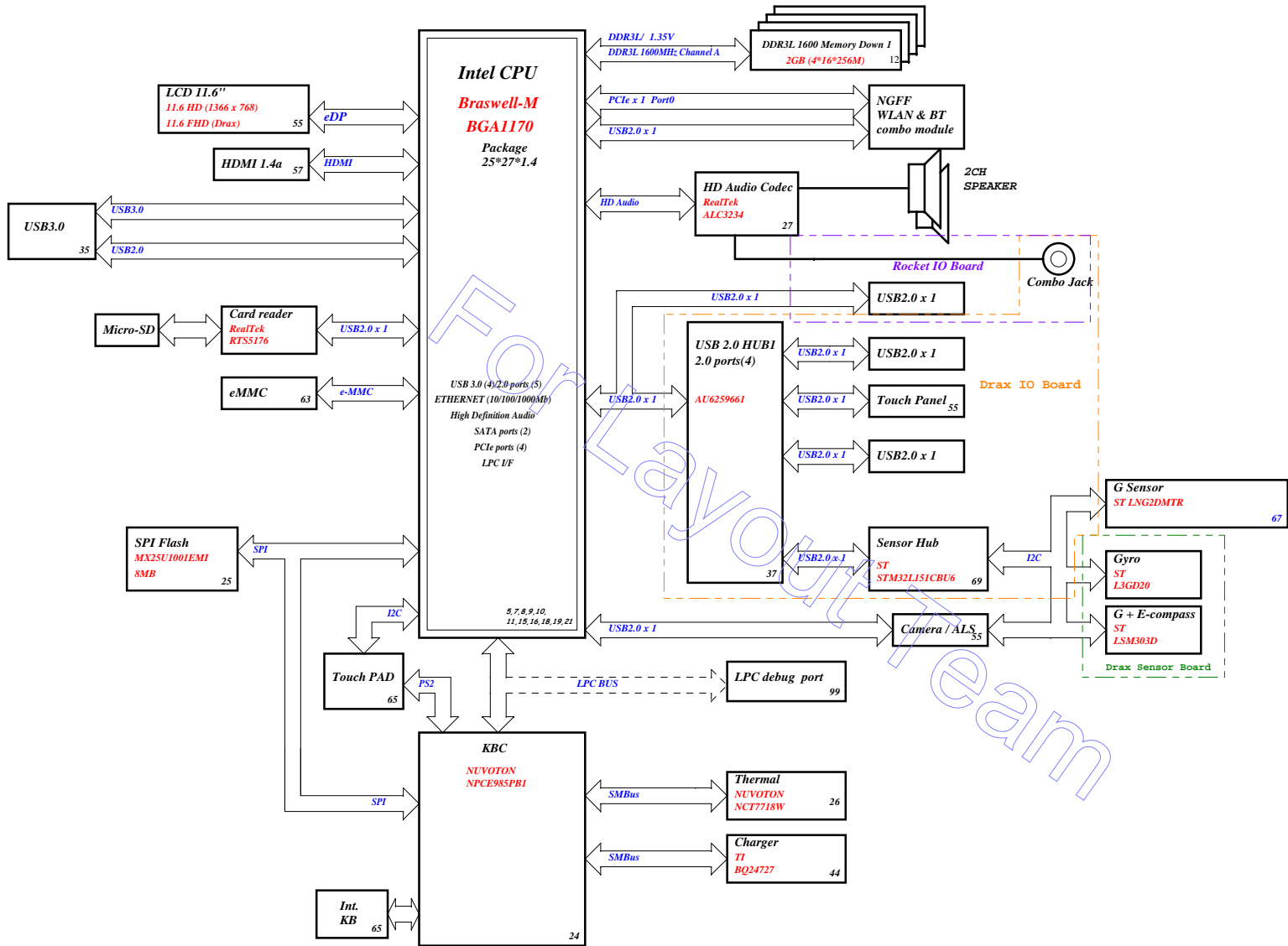
Rev  
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Date: Monday, November 09, 2015

Sheet 1 of 109

Project code : 4PD076010001  
PCB P/N : 15235  
Revision : -1

Rocket 11.6" Block Diagram - 0SP



CHARGER	
BQ24727R0RR	44
INPUTS	OUTPUTS
19V_AD+	12V_BT+
SYSTEM DC/DC	
SY8288CRAC	45
SY8286BRAC	
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_AUX_S5
	5V_S5
CPU DC/DC	
NCP81201MNTXG	46-47
INPUTS	OUTPUTS
19V_DCBATOUT	1V_CPU_CORE
CPU DC/DC	
NCP81201MNTXG	48
INPUTS	OUTPUTS
19V_DCBATOUT	6FX_CORE
SYSTEM DC/DC	
SY8286RAC	50
INPUTS	OUTPUTS
19V_DCBATOUT	1D05V_S5
Step Down Regulator	
SYW232DFC	50
INPUTS	OUTPUTS
3D3V_S5	1D15V_S5
SYSTEM DC/DC	
SY8286RAC	51
INPUTS	OUTPUTS
19V_DCBATOUT	1D35V_CPU_VDDQ_S3
SYSTEM DC/DC	
APL5338XAI	51
INPUTS	OUTPUTS
1D35V_CPU_VDDQ_S3	0D675V_VREF_S0
Step Down Regulator	
SYW232DFC	52
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
SYSTEM LDO	
S-1339D15-M5001	53
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
SYSTEM LDO	
APL5930KAI	54
INPUTS	OUTPUTS
3D3V_S5	1D24V_S5


PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

SSID = CPU

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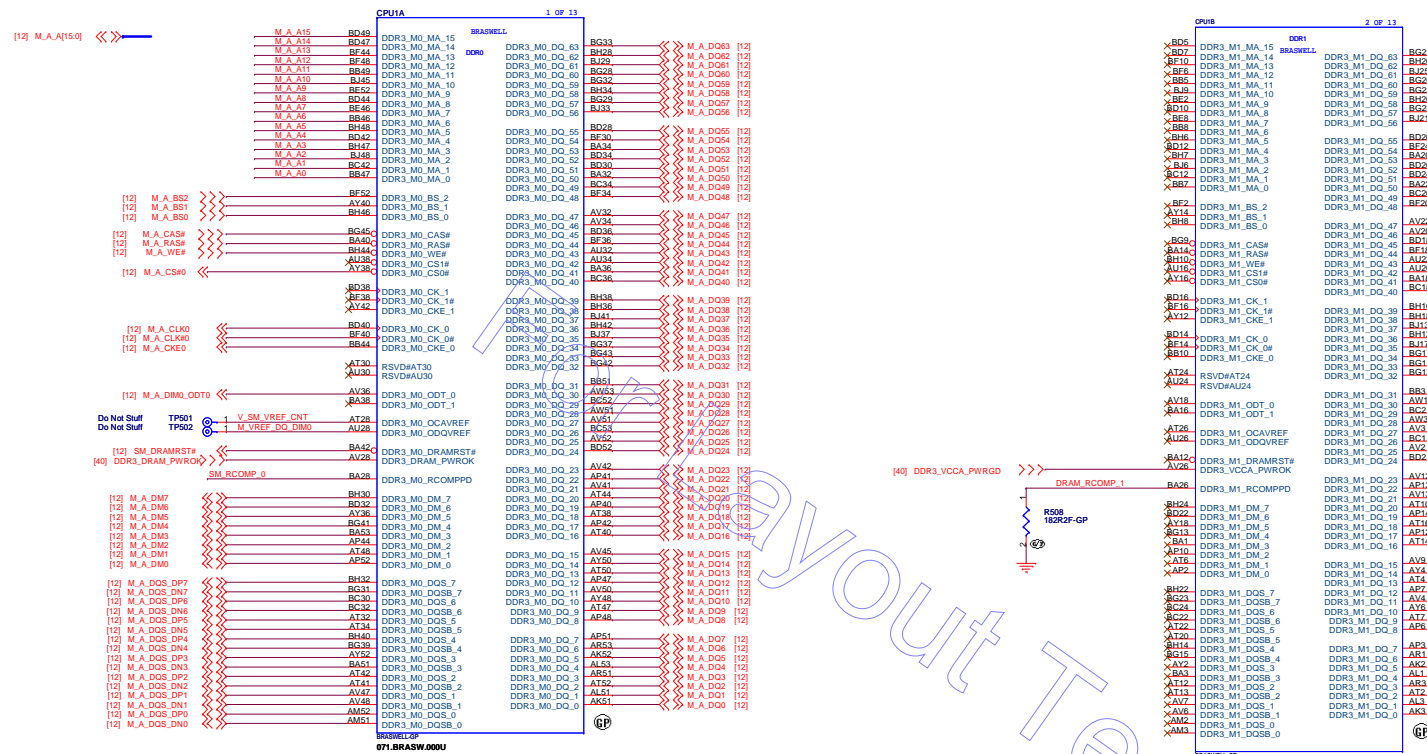
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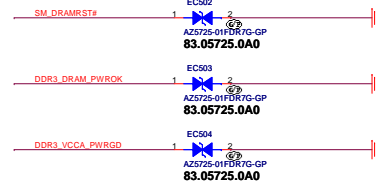
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Layout Note: Close CPU

## Follow Intel Check List, Remove Reference Voltage

DDR3_M0_ODQVREF DDR3_M1_ODQVREF	Not applicable to DDR3L implementation. In DDR3L mode, these pins are No Connect on SoC Vref. External Vref circuitry needs to be given on SODIMM side. Example shown as below 0.5*VCCDDR_1P24_1P35. Use 1% resistor. Cannot go higher than 0.6*VCCDDR_1P24_1P35. Example shown as below	Not use for DDR3L design.
DDR3_M0_OCAVREF DDR3_M1_OCAVREF	Not applicable to DDR3L implementation. In DDR3L mode, these pins are No Connect on SoC Vref. External Vref circuitry needs to be given on SODIMM side. Example shown as below 0.5*VCCDDR_1P24_1P35. Use 1% resistor. Cannot go higher than 0.6*VCCDDR_1P24_1P35. Example shown as below	Not use for DDR3L design.



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SSID = CPU

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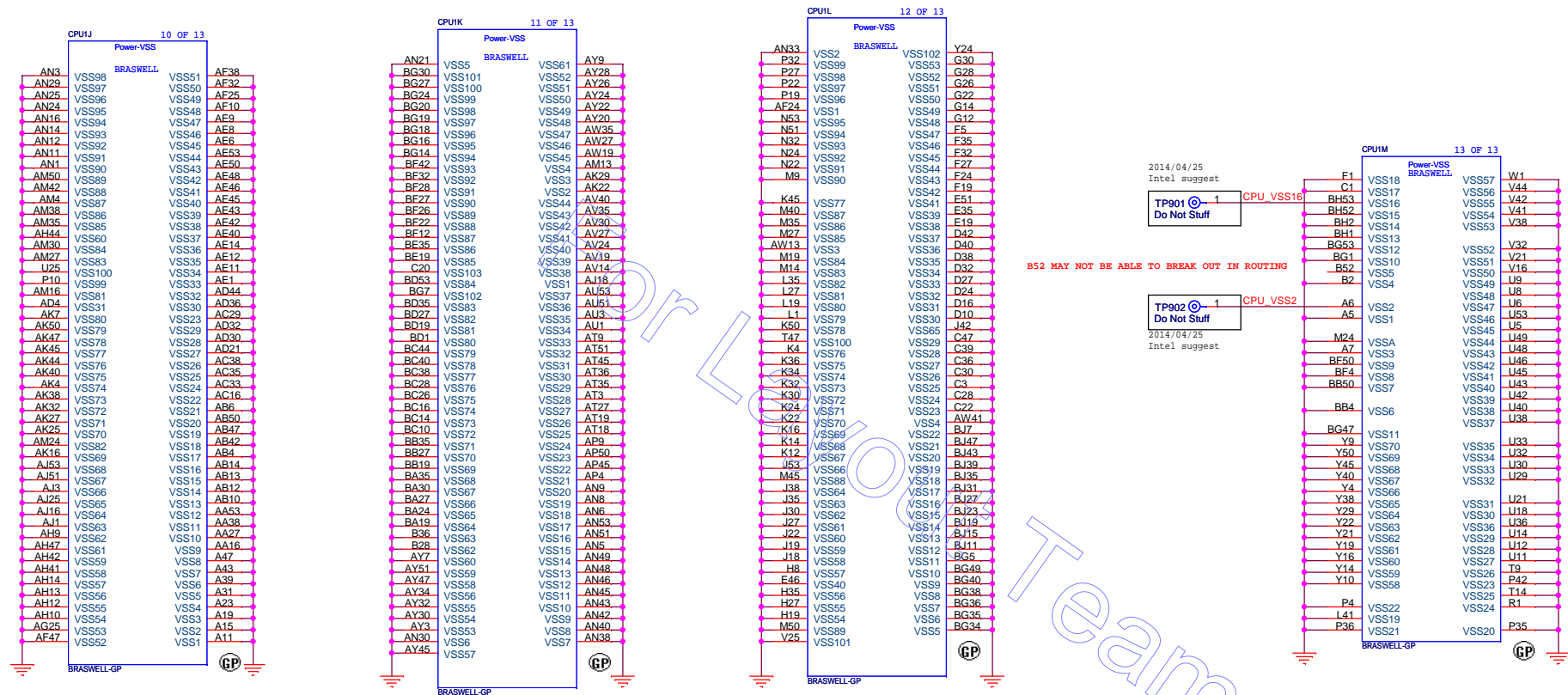
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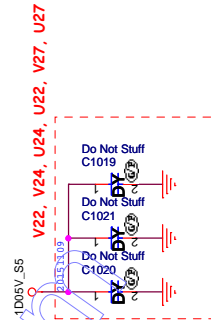
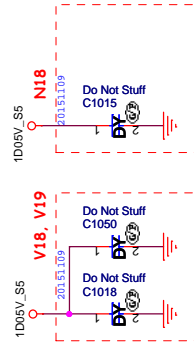
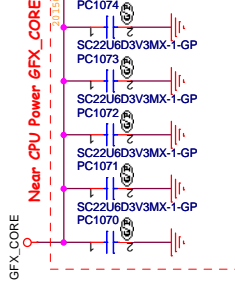
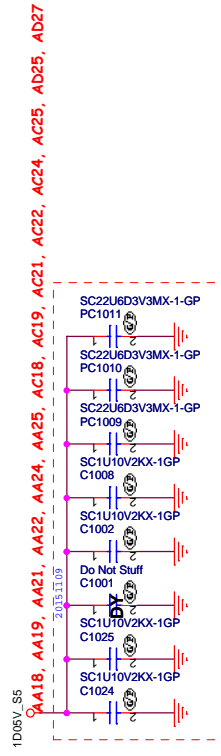
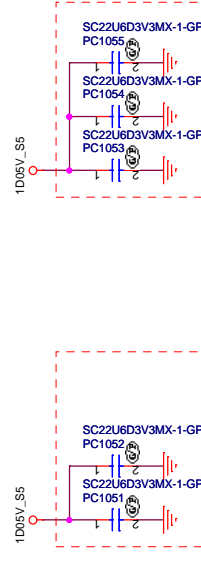
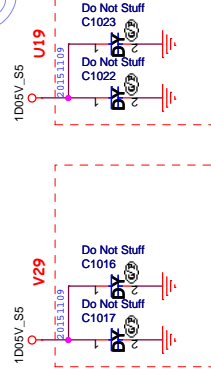
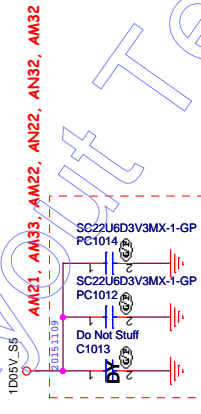
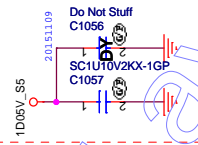
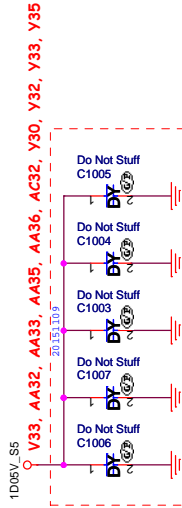
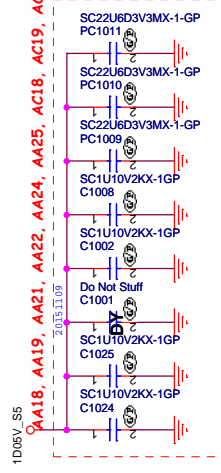
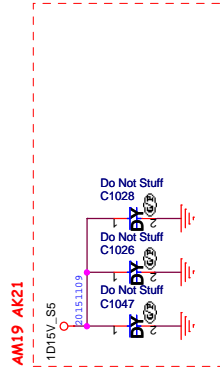
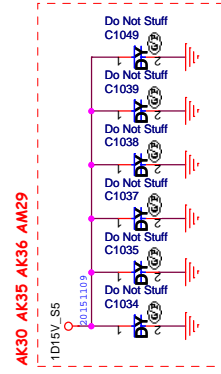
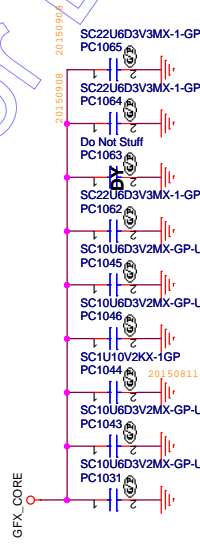
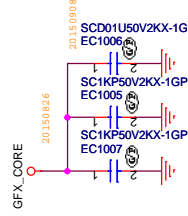
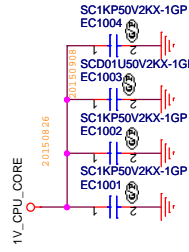
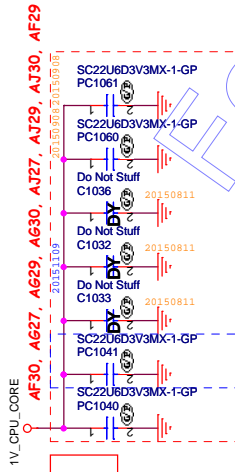
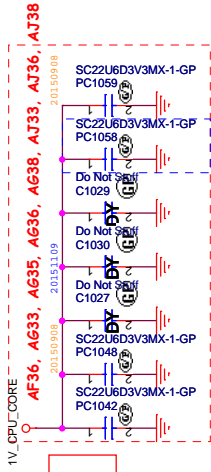
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CPU (VSS)		
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Date:	Monday, November 16, 2015	Sheet 9 of 109

SSID = CPU

PLACE ALL THE CAPS  
UNDER THE PKG SHADOW

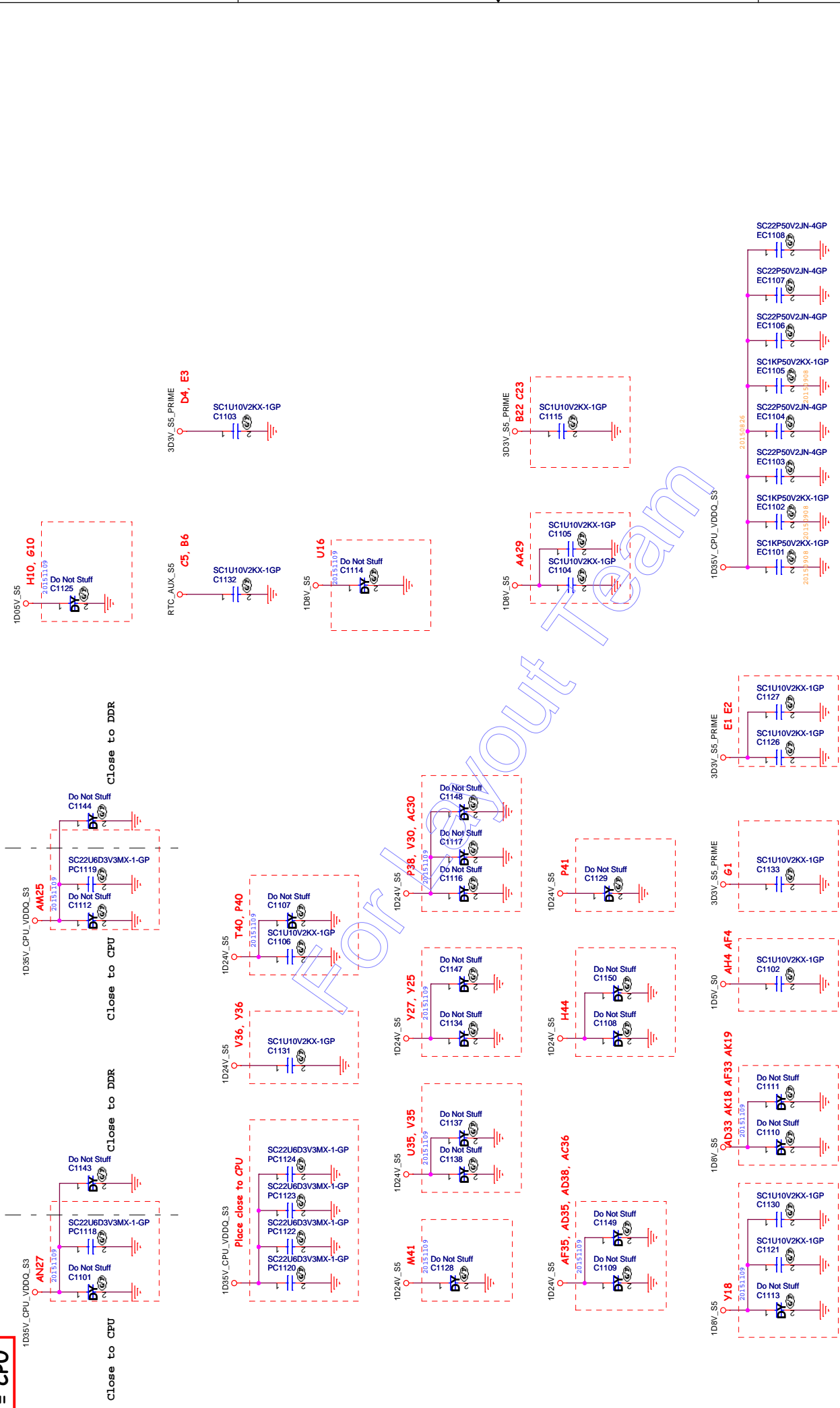
PLACE ALL THE CAPS  
UNDER THE PKG SHADOW



PLACE CLOSE TO PIN 1 OF RA

PLACE CLOSE TO PIN 1 OF RB

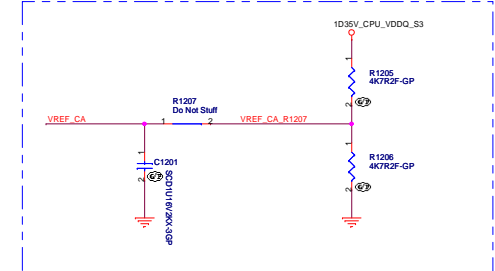
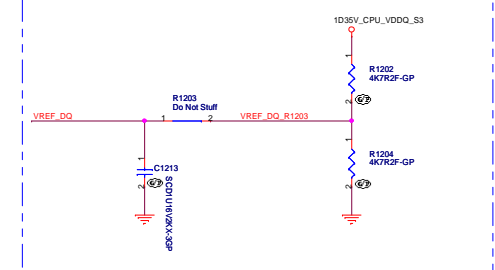
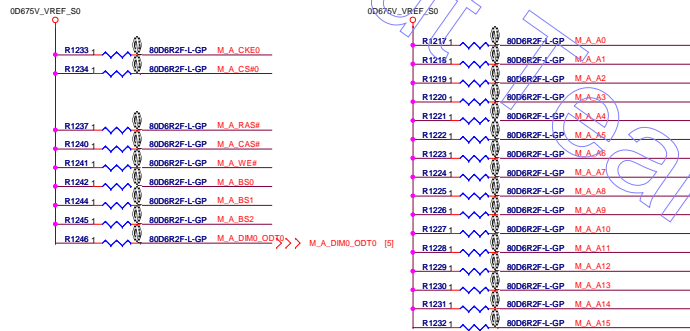
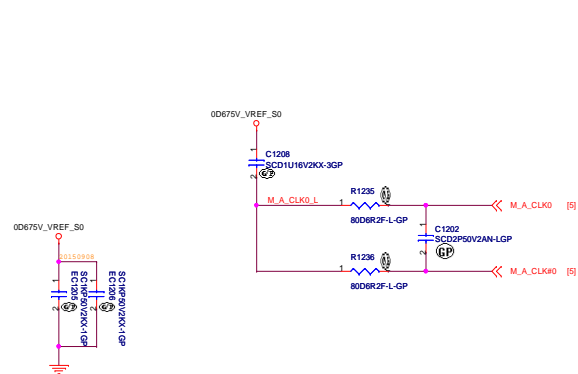
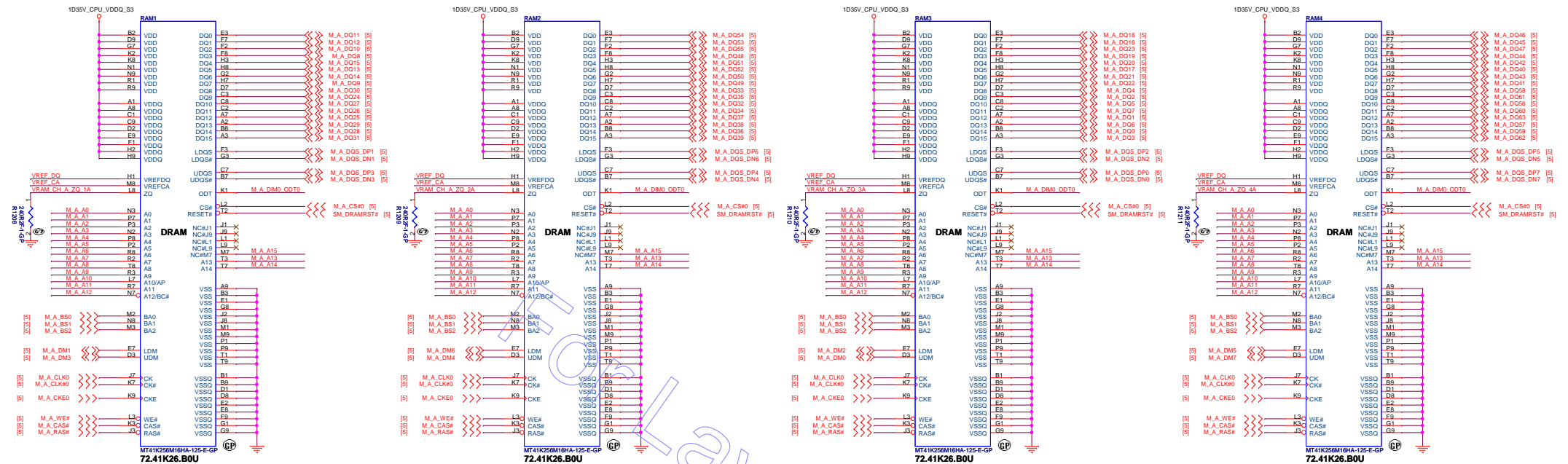
SSID = CPU



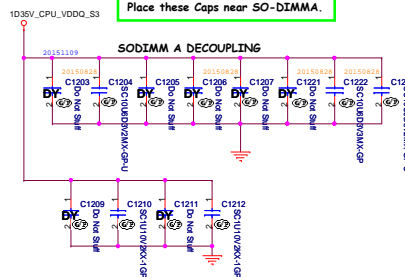
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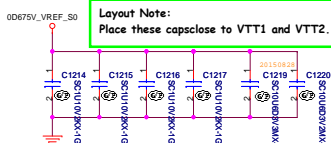
## SSID = MEMORY



Layout Note:  
Place these Caps near SO-DIMMA.



Layout Note:  
Place these caps close to VTT1 and VTT2.




Reserve 0.1uF for ESD

SSID = MEMORY

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SSID = CPU

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Date: Monday, November 09, 2015		Sheet 14 of	109

SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC  
SHOULD BE PLACED OUTSIDE KOZ AREA

All the straps are sampled on the rising edge of the  
PMC\_RSMRST\_N signal (check list)

Description	DDI0_Detected	DDI1_Detected	A16 Swap Override	DSI Display Detected	Boot BIOS Strap BBS	Flash Descriptor Security Override	DFX Boot Halt Strap & VISA Early POSM Debug Enable	DFX Sus Debug Strap	ICLK, USB2, DDI SFR Supply Select	ICLK SFR Bypass	POSM Select	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC bypass
GPIO	GPIO_SUS0	GPIO_SUS1	GPIO_SUS2	GPIO_SUS3	GPIO_SUS4	GPIO_SUS5	GPIO_SUS6	GPIO_SUS7	SEC_GPIO_SUS8	SEC_GPIO_SUS9	SEC_GPIO_SUS10	GP_CAMERASB08	GP_CAMERASB09	GP_CAMERASB11
Schematic														
High	DDI0 Detect	DDI1 Detect	Normal Operation	DSI Detect	Boot from SPI	Weak internal pull-up Normal Operation	Normal	Weak internal pull-up Normal	1.35V	Weak internal pull-up Bypass with 1.05V	PMC	Bypass	Bypass	Bypass
Low	Disable	Disable	Change Boot Loader address (A16 Override)	Disable	Boot from LPC	Override	Halt boot enable	Sus Debug enable	1.25V	No bypass	Fuse controller	No bypass	No bypass	No bypass

Table 29. Straps (Sheet 1 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal pull-down	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal pull-down	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	A16 swap override	Weak internal pull-up	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull-up	BIOS Boot Selection 0 = - 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull-up	Security Flash Descriptors 0 = Override 1 = Normal Operation

Table 29. Straps (Sheet 2 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull-down	0 = Supply is 1.25V 1 = Supply is 1.35V This strap also contains PLL LDO 0: supply is 1.25V; 1: supply is 1.35V. Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, ICLK and DDI
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull-up	0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[10]	POSM Select	Weak internal pull-down	Selects which POSM will be observed at time 0 0 = Fuse controller 1 = PMC
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass

CHV Straps [CRB] -- strap detect @ RSMRST# assertion				
Purpose	CHV Pin Name (refer CHV symbol PIN)	PU/PD (internal - Weak)	Options	Default State on board?
DDI0 Detected	GPIO_SUS0	PD	1 - DDI0 Detect, 0 - Disable	High
DDI1 Detected	GPIO_SUS1	PD	1 - DDI1 Detect, 0 - Disable	High
A16 swap override	GPIO_SUS2	PU	1 - Default, 0 - A16 override	High
DSI Display Detected	GPIO_SUS3	PD	1 - DSI detect, 0 - Disable	Low
Boot BIOS Strap BBS	GPIO_SUS4	PU	1 - Boot from SPI, 0 - Boot from LPC	High
Flash Descriptor Security Override	GPIO_SUS5	PU	1 - Security enabled, 0 - Security disabled	High
DFX Boot Halt Strap & VISA Early POSM Debug Enable	GPIO_SUS6	PU	1 - normal, 0 - Halt boot enable	High
DFX Sus Debug Strap	GPIO_SUS7	PU	1 - Normal, 0 - Sus Debug enable	High
ICLK, USB2, DDI SFR Supply Select	SEC_GPIO_SUS8	PU	1 - 1.35V, 0 - 1.25V	Low
ICLK SFR Bypass	SEC_GPIO_SUS9	PD	1 - Bypass with 1.05V, 0 - No Bypass	Low
POSM Select	SEC_GPIO_SUS10	PD	1 - PMC, 0 - Fuse controller	Don't care, if GPIO_SUS6 is pulled high.
ICLK Xtal OSC Bypass	GP_CAMERASB08	PD	1 - Bypass, 0 - No bypass	Low
CCU SUS RO Bypass	GP_CAMERASB09	PD	1 - Bypass, 0 - No bypass	Low
RTC OSC Bypass	GP_CAMERASB11	PD	1 - Bypass, 0 - No bypass	Low








SSID = CPU

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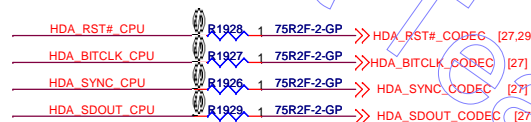
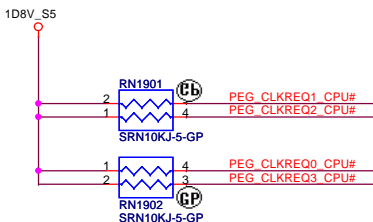
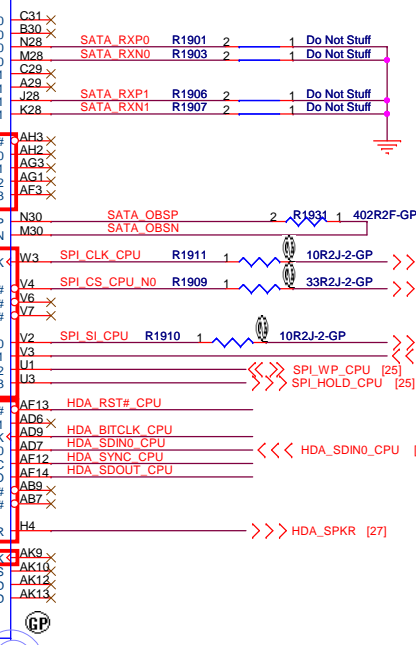
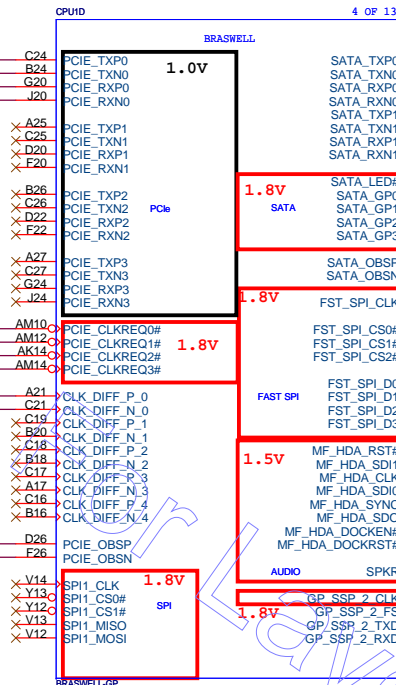


SSID = PCH

WLAN

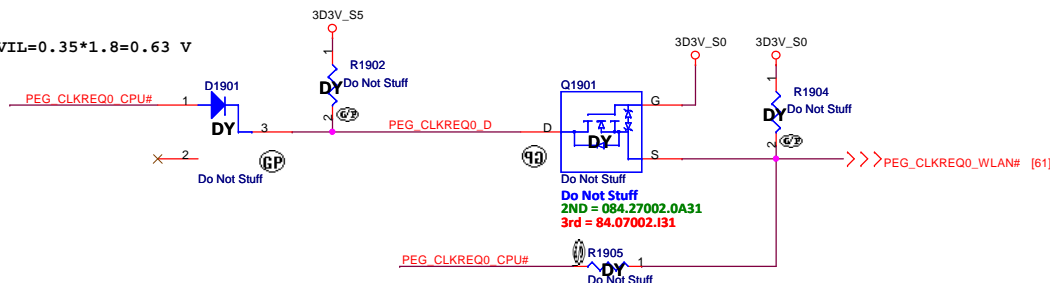
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C1915 2  
C1916 2  
SCD1U16V2KX-3GP  
PCIE\_TX\_CPU\_P0  
PCIE\_TX\_CPU\_N0



Remove?

$VIL = 0.35 \times 1.8 = 0.63 \text{ V}$



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CPU (SATA/PCIE/IHDA)

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Sheet 19 of 109

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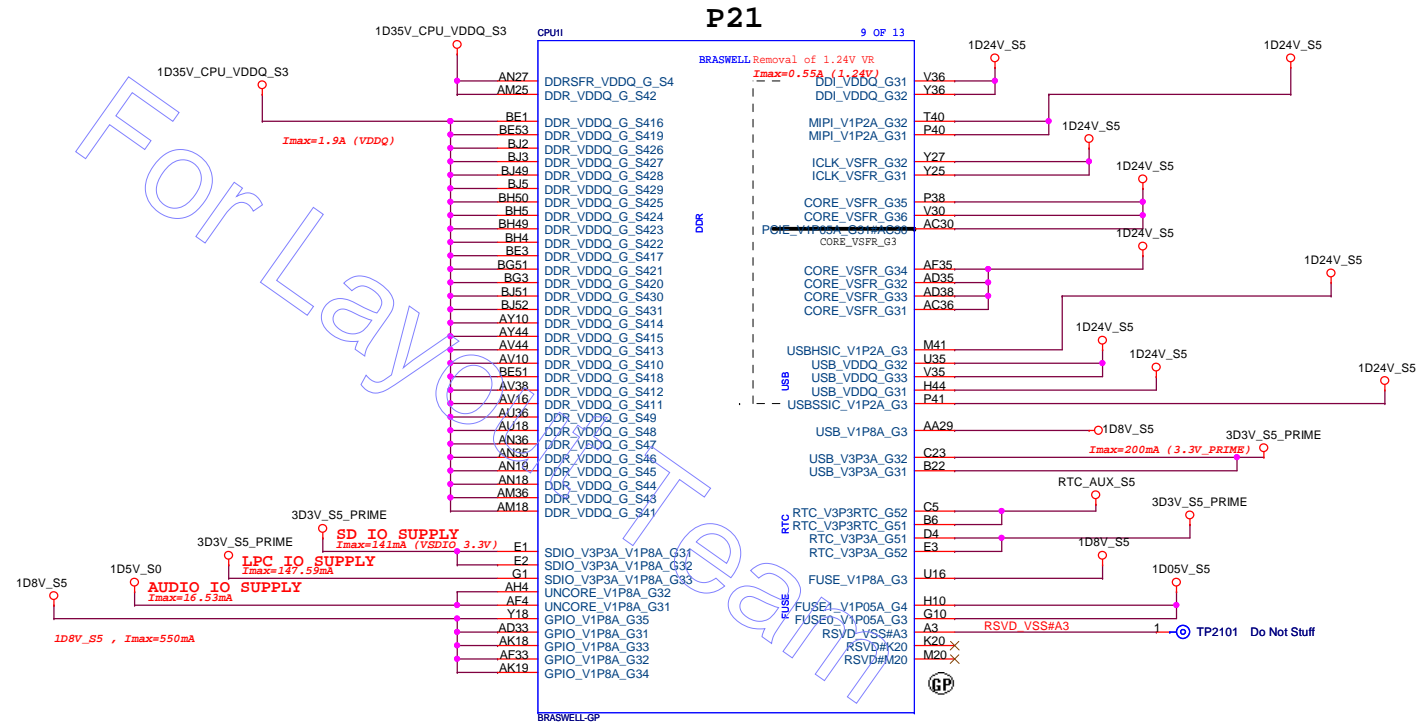
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Sheet 22 of 109

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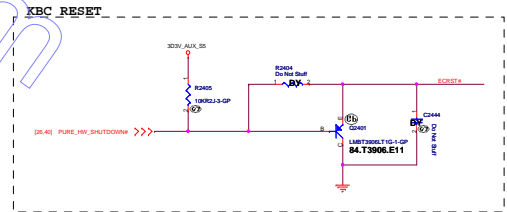
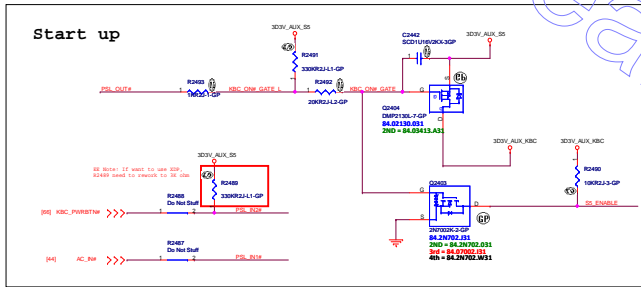
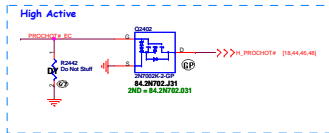
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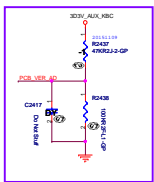
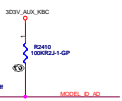
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Sheet 23 of 109



	Rocket	Drax
ID	1	0



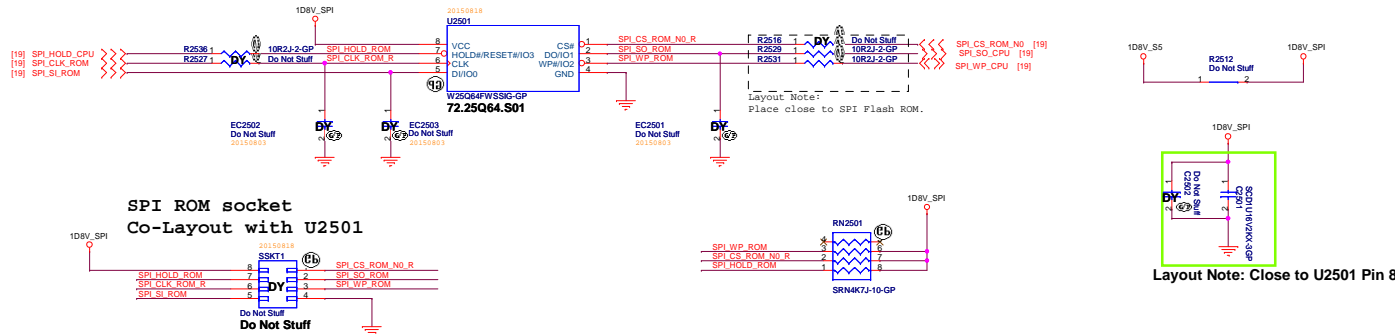
ASIC Model	Full-Size Register	Full-size Register	Typical Voltage	Max Voltage	Max Voltage	ASIC Firmware Setting
SA	100.0 K	100.0 K	3.000 V	3.050 V	2.940 V	>+2.95 V
SC	100.0 K	200.0 K	2.750 V	2.750 V	2.740 V	>+2.616 V <+2.875 V
SB	100.0 K	33.0 K	2.481 V	2.405 V	2.468 V	>+2.363 V <+2.616 V
-1	100.0 K	47.0 K	2.345 V	2.250 V	2.295 V	>+2.123 V <+2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.019 V	1.954 V	>+1.934 V <+2.123 V
Reserved for project use	100.0 K	75.3 K	1.957 V	1.870 V	1.870 V	>+1.780 V <+1.954 V
Reserved for project use	100.0 K	100.0 K	1.858 V	1.862 V	1.838 V	>+1.740 V <+1.740 V
Reserved for project use	100.0 K	143.3 K	1.558 V	1.542 V	1.543 V	>+1.201 V <+1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	2.1297 V	1.181 V	>+1.126 V <+1.201 V
Reserved for project use	100.0 K	215.0 K	1.043 V	1.0520 V	1.0354 V	>+0.524 V <+1.126 V





SSID = Flash.ROM

## SPI FLASH ROM (8M byte) for CPU



## SPI ROM link to KBC



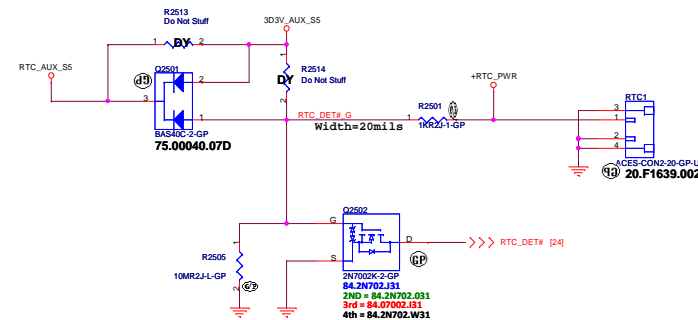
## High Speed Switch for Share ROM

5240626:SPI Signals do not get tri-stated / MUX Sol.

Truth Table

OE#	S	D+	D-	Function
H	X	Hi-Z	Hi-Z	Disable
L	L	1D+	1D-	D=1D
L	H	2D+	2D-	D=2D

SSID = RTC

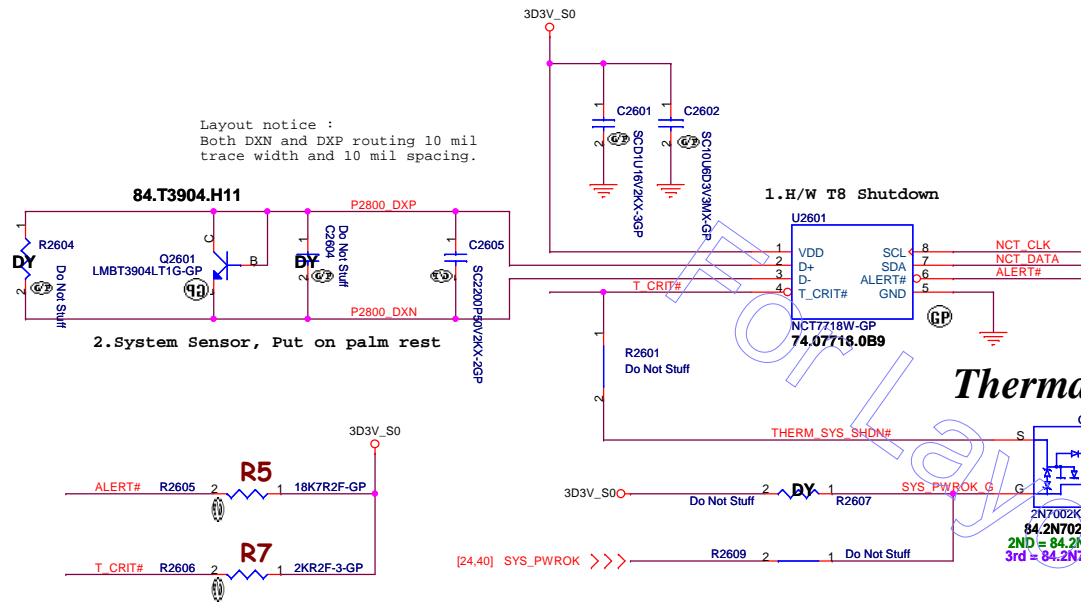


Rocket BSW 1st

SSID = Thermal

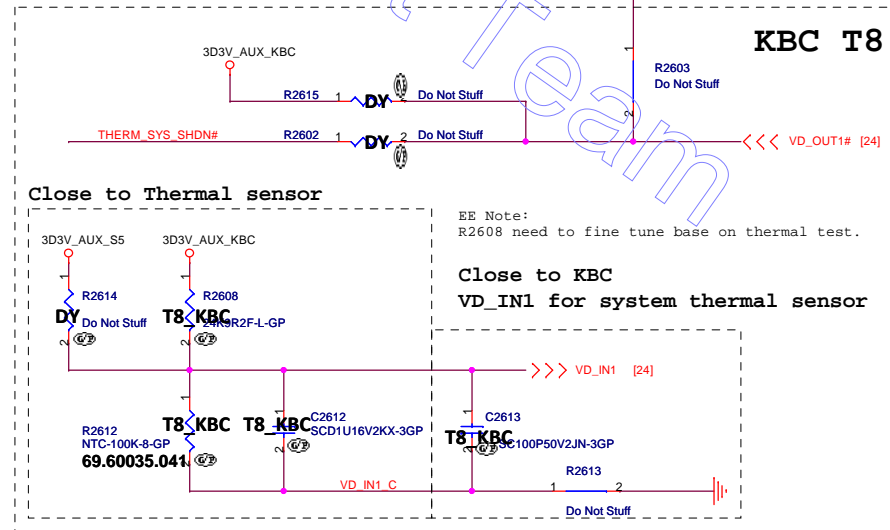
1. T8: PURE\_HW\_SHUTDOWN# through Q2603.
2. THM\_SENSOR: Thermal sensor NCT7718W solution.

Layout notice :  
Both DXN and DXP routing 10 mil  
trace width and 10 mil spacing.

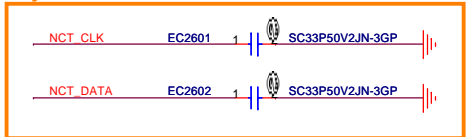


The default value is trapping after power up 100ms by different pull-up resistors of T\_CRIT# and ALERT# pin:

TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



**Layout Note: Close U2601**



pull-high at p.24  
(3D3V\_S5)

N# [24,40]

KBC T8

Close to Thermal sensor

EE Note:  
R2608 need to fine tune base on thermal test.

Close to KBC  
VD\_IN1 for system thermal sensor

Rocket BSW 1st



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[illegible]

### **Thermal**

Size  
A3

Document Number
-----------------

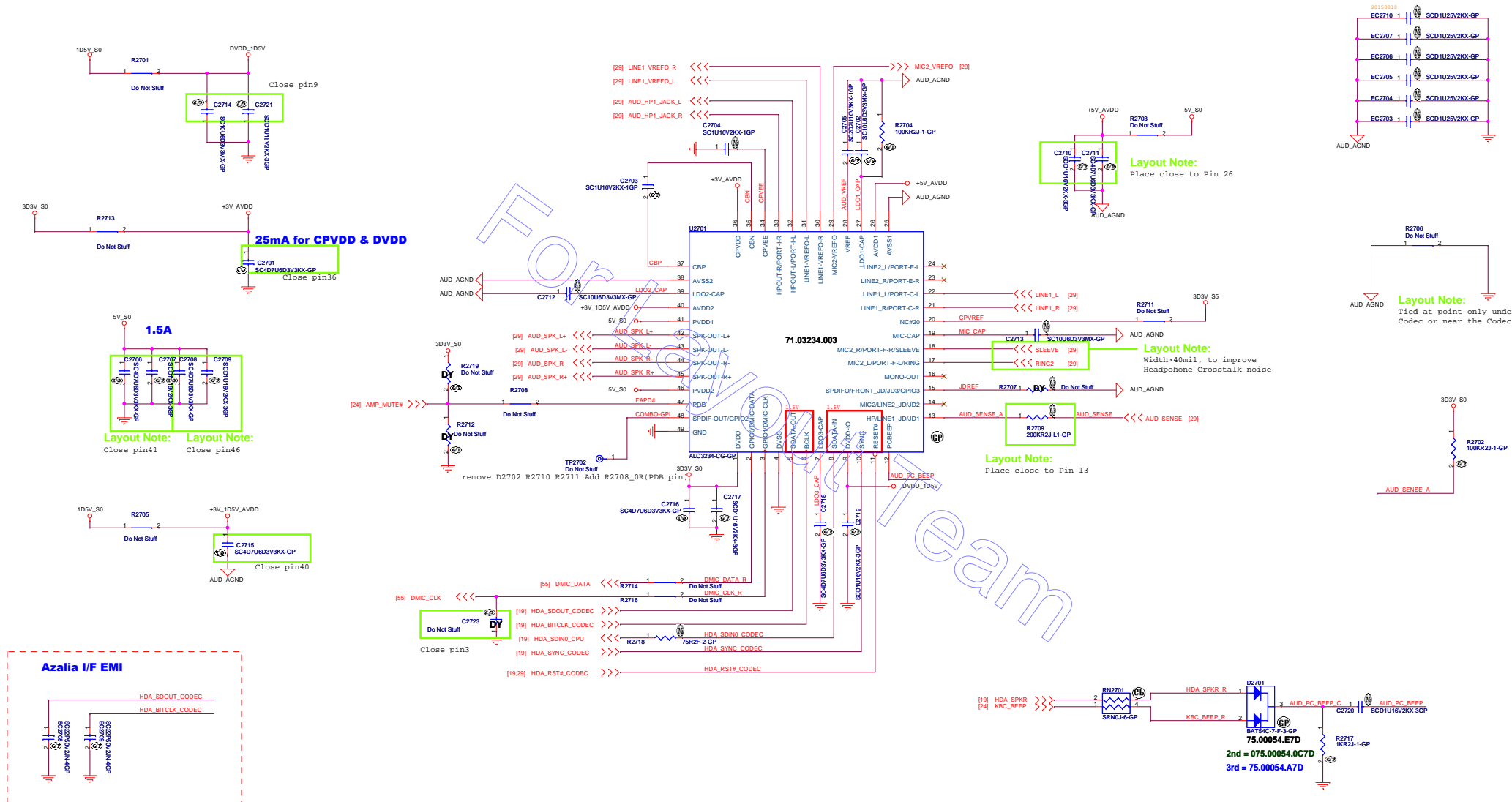
**Rocket BSW 11.6"**

Rev	
<b>A00</b>	

Date: Monday, November 09, 2015

Sheet	26	of	109
-------	----	----	-----

SSID = AUDIO



# Blanking

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Title

**(Reserved)**

Size  
A4

Document Number

**Rocket BSW 11.6"**

Rev  
**A00**

Date: Monday, November 09, 2015

Sheet 28 of 109



SSID = LOM

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Title

**(Reserved)LOM**

Size  
A4

Document Number

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Rev  
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Date: Monday, November 09, 2015


Sheet 30 of 109

SSID = LAN

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Title (Reserved)LAN			
Size A4	Document Number Rocket BSW 11.6"		Rev A00
Date: Monday, November 09, 2015		Sheet 31 of 109	

SSID = LAN CONN

Blanking

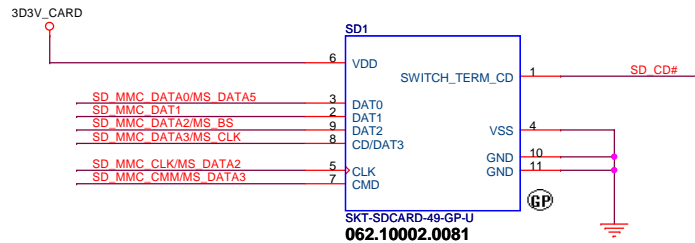
For Layout Team

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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>(Reserved)RJ45+Transformer</b>		
Size A4	Document Number <b>Rocket BSW 11.6"</b>	Rev <b>A00</b>
Date: Monday, November 09, 2015		Sheet 32 of 109

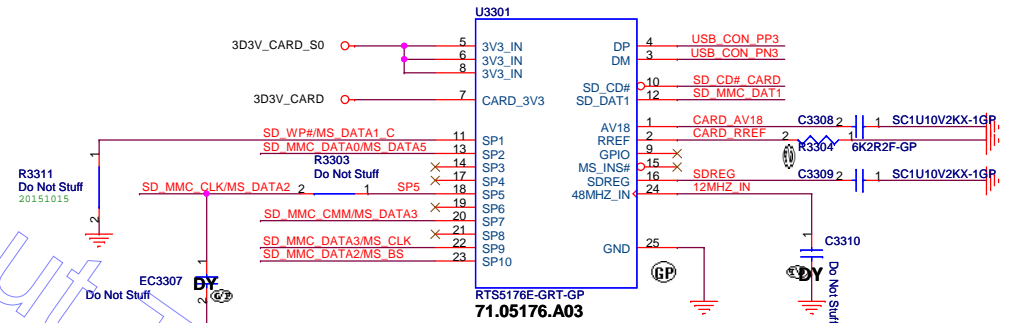
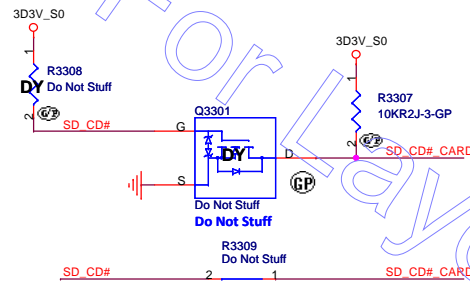
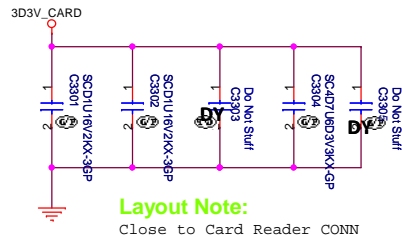


# SSID = Card Reader

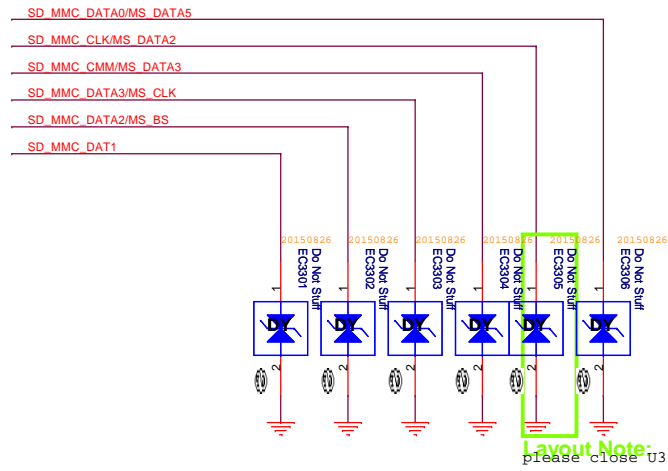


## SD Card Connector

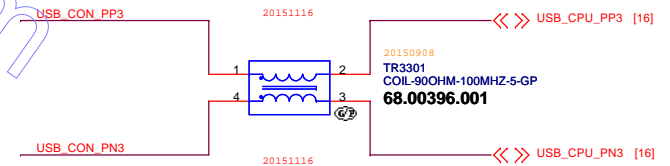
Pin	Define
P1	SWITCH TERM CD
P2	DAT1
P3	DAT0
P4	VSS
P5	CLK
P6	VDD
P7	CMD
P8	CD/DAT3
P9	DAT2
P10	GND
P11	GND



## For EMI Reserved



Pin name	Net name
SD_DAT1	SD MMC_DAT1
SP1	SD_WP/MS_DATA1
SP2	SD MMC_DATA0/MS_DATA5
SP3	MMC_DATA7/MS_DATA4
SP4	MMC_DATA6/MS_DATA0
SP5	SD MMC_CLK/MS_DATA2
SP6	MMC_DATA5/MS_DATA6
SP7	SD MMC Command/MS_DATA3
SP8	MMC_DATA4/MS_DATA7
SP9	SD MMC_DATA3/MS_CLK
SP10	SD MMC_DATA2/MS_BS



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Title			Card Reader + CONN	
Size	Document Number	Rev		A00
A3	Rocket BSW 11.6"			
Date:	Monday, November 16, 2015	Sheet	33	of 109

SSID = USB

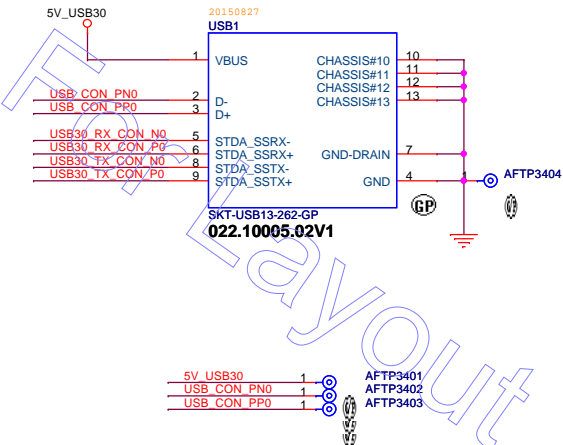
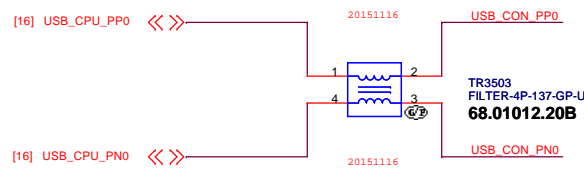
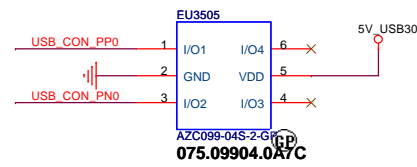
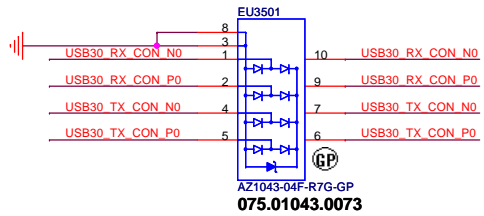
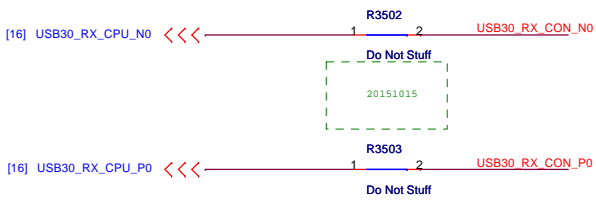
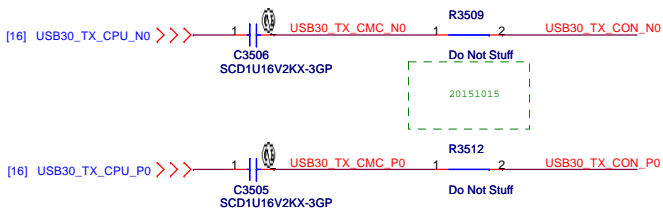
Blanking

For Layout Team

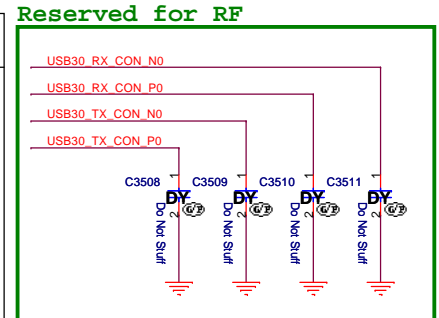
Rocket BSW 1st

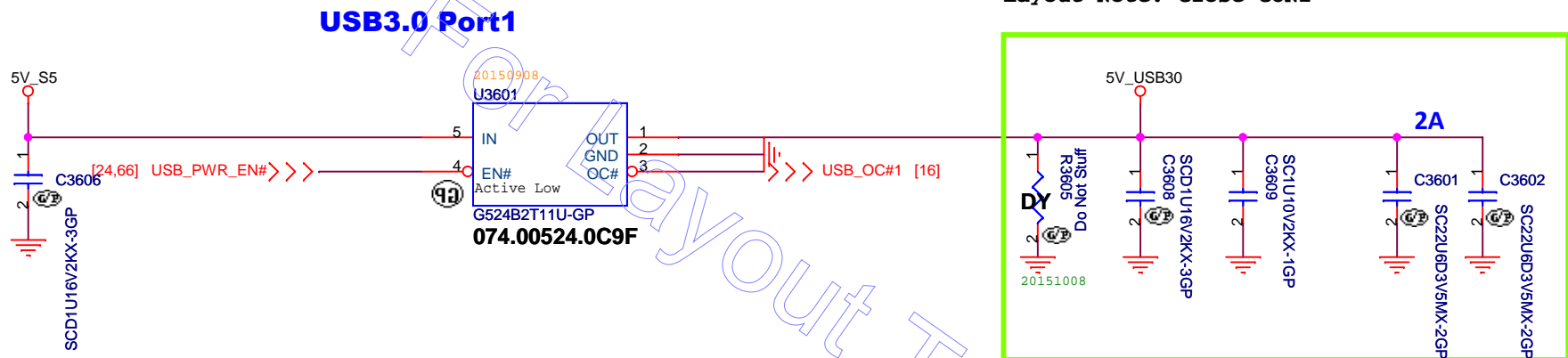
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)USB 2.0 Port</b>			
Size A4	Document Number <b>Rocket BSW 11.6"</b>		Rev <b>A00</b>
Date: Monday, November 09, 2015		Sheet 34	of 109

SSID = USB




USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+





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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> <b>USB Power SW</b>			
Size A4	Document Number <b>Rocket BSW 11.6"</b>		Rev <b>A00</b>
Date: Monday, November 09, 2015		Sheet 36 of	109

SSID = USB

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Title

**USB2.0 HUB**

Size  
A4

Document Number

**Rocket BSW 11.6"**

Rev  
**A00**

Date: Monday, November 09, 2015

Sheet 37 of 109

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Title

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A4

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Rev  
**A00**

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Sheet 38 of 109

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Title

**(Reserved)**

Size  
A4

Document Number

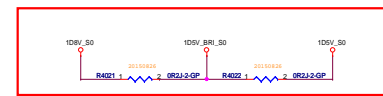
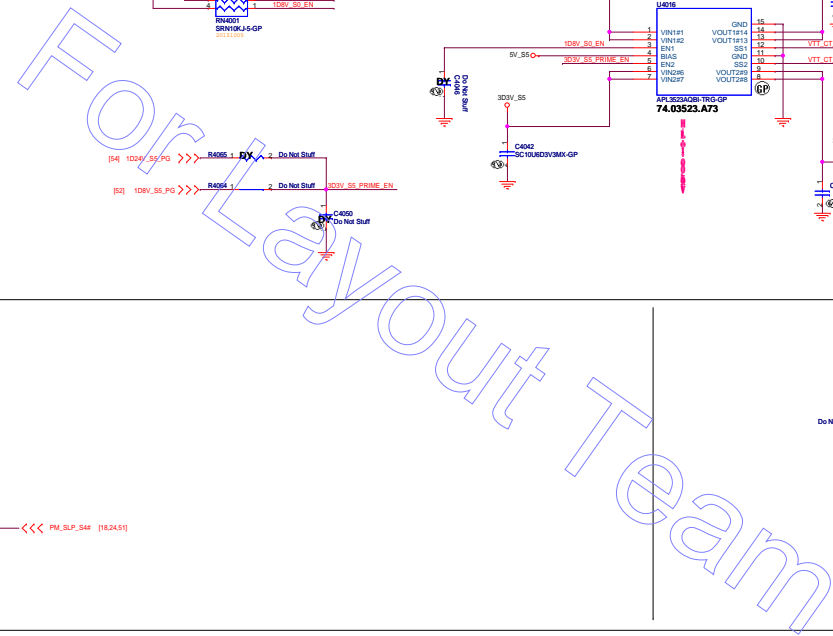
**Rocket BSW 11.6"**

Rev  
**A00**

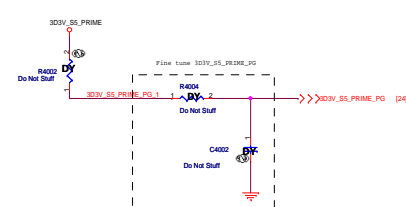
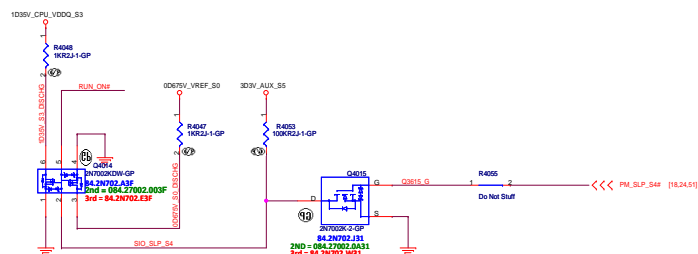
Date: Monday, November 09, 2015

Sheet 39 of 109

### Power Sequence



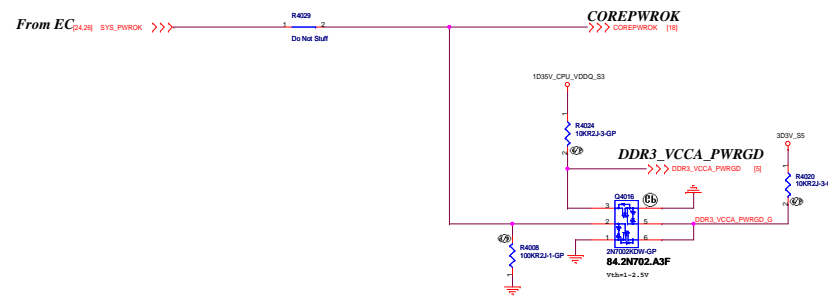
### *Discharge circuit*



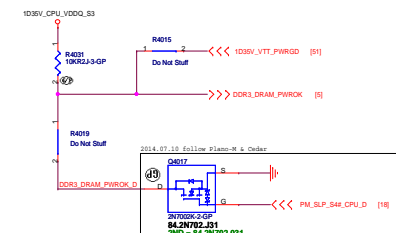
---

### *Power Sequence*

***DDR3\_VCCA\_PWRGD***



***DDR3\_DRAM\_PWROK***






# Blanking

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Title <b>(Reserved)</b>			
Size A4	Document Number <b>Rocket BSW 11.6"</b>		Rev <b>A00</b>
Date: Monday, November 09, 2015		Sheet 41 of	109

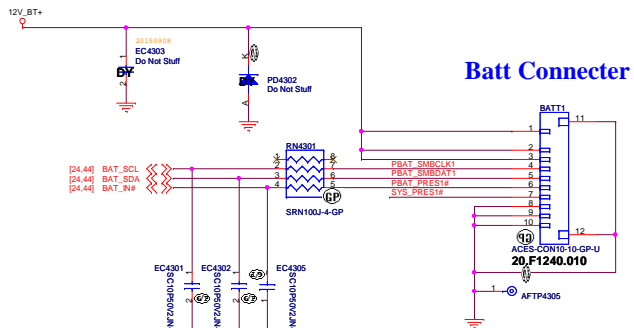
# Blanking

For Layout Team

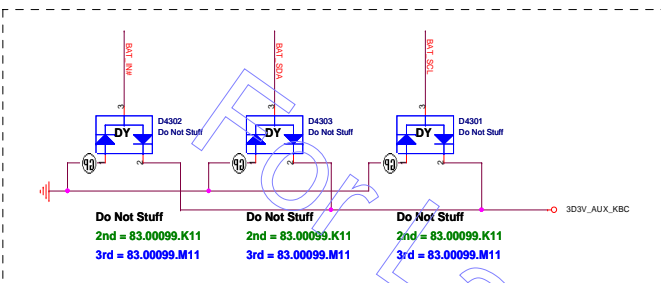
Rocket BSW 1st

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Title <b>(Reserved)</b>			
Size A4	Document Number <b>Rocket BSW 11.6"</b>		Rev <b>A00</b>
Date: Monday, November 09, 2015		Sheet 42 of	109

```
SSID = PWR.Support
```



Placement: Close to Batt Connector



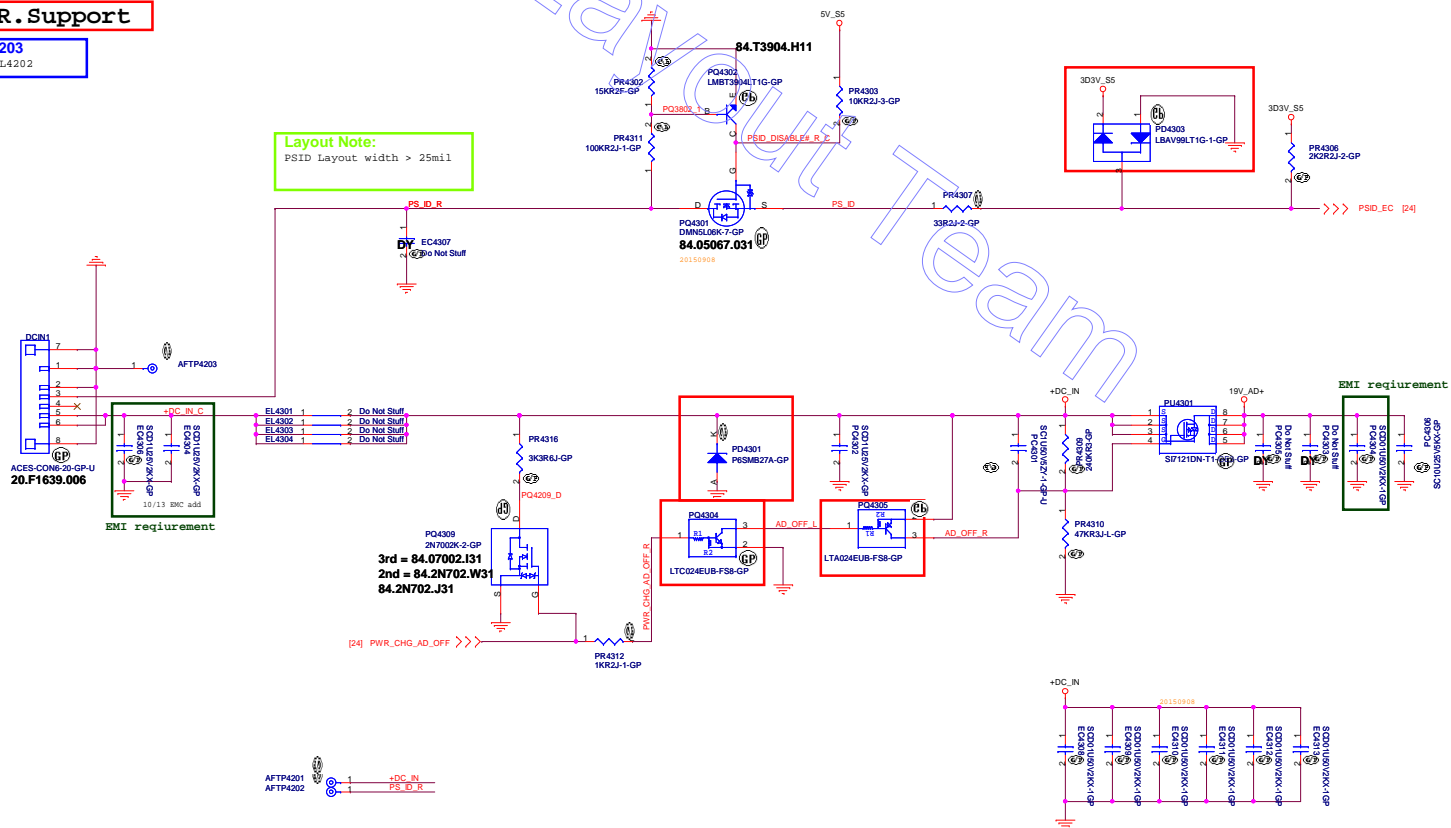
```
SSID = PWR.Support
```

0103 Add EC4203

ndde close to EL4202

**Layout Note:**

PSID Layout width > 25mil



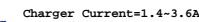
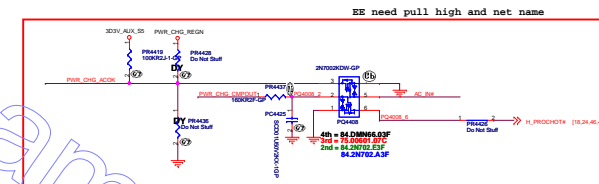
**Rocket BSW 1st**

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Title **BATTERY CONN**

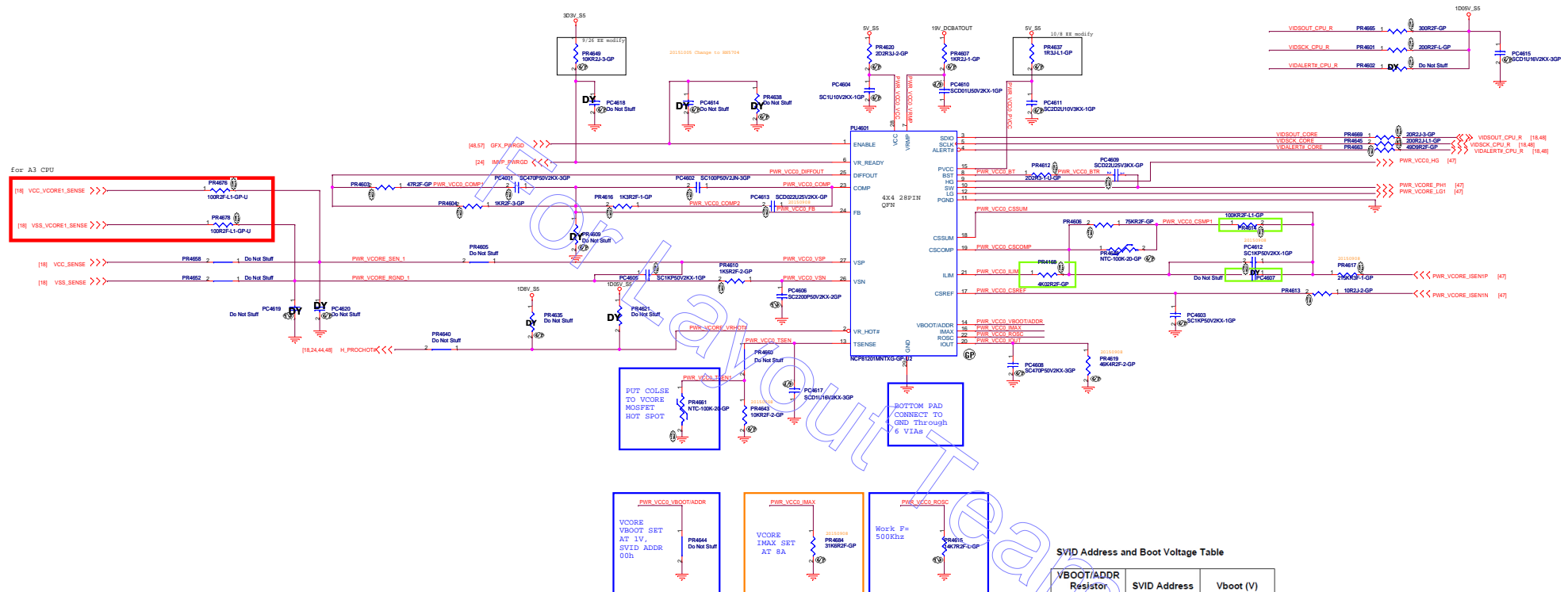
Size A2	Document Number <b>Rocket BSW 11.6"</b>	Rev <b>A00</b>
Date: Monday, November 09, 2015	Sheet 43 of	109

Main Func = Charger

[illegible]



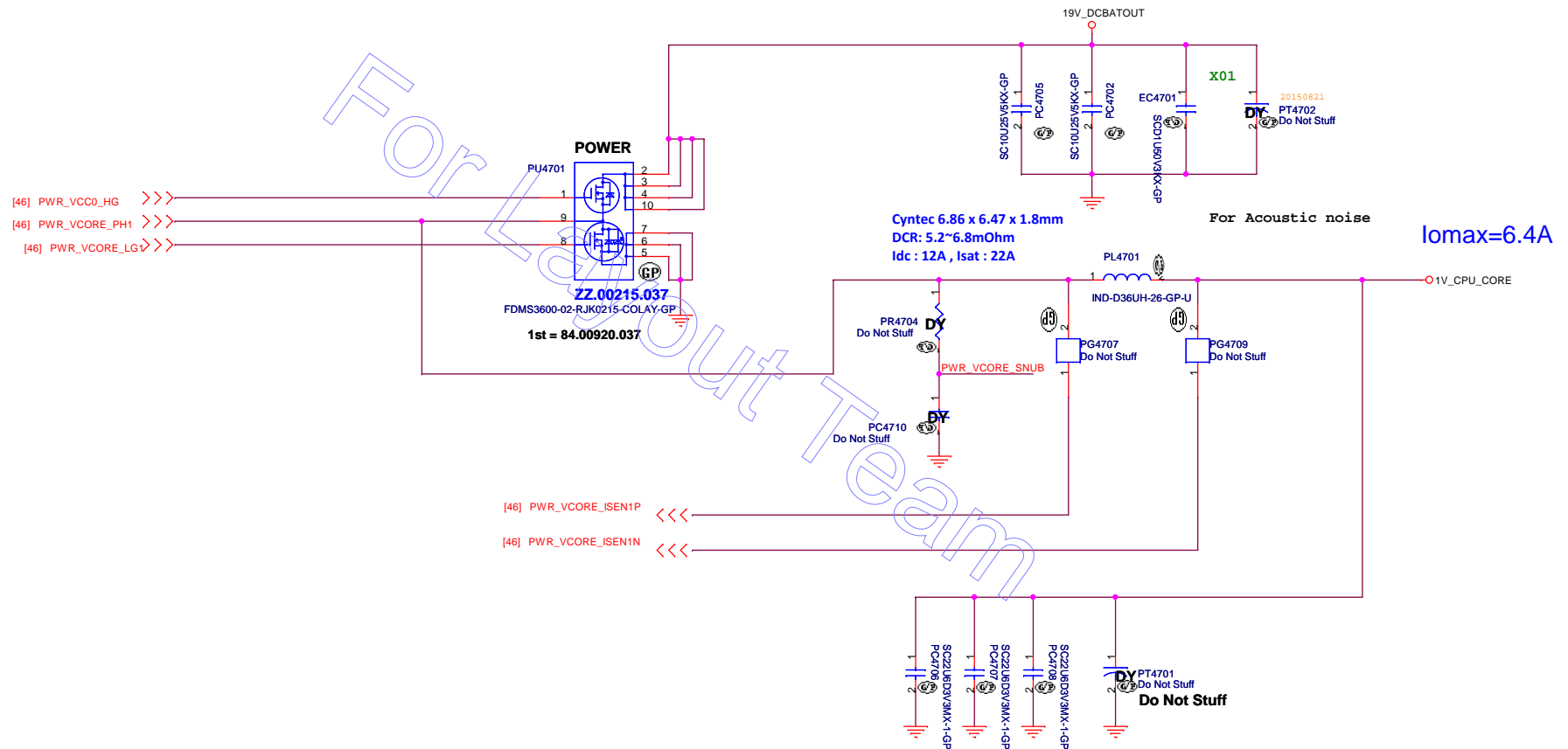
SSID = CPU Regulator



### SVID Address and Boot Voltage Table

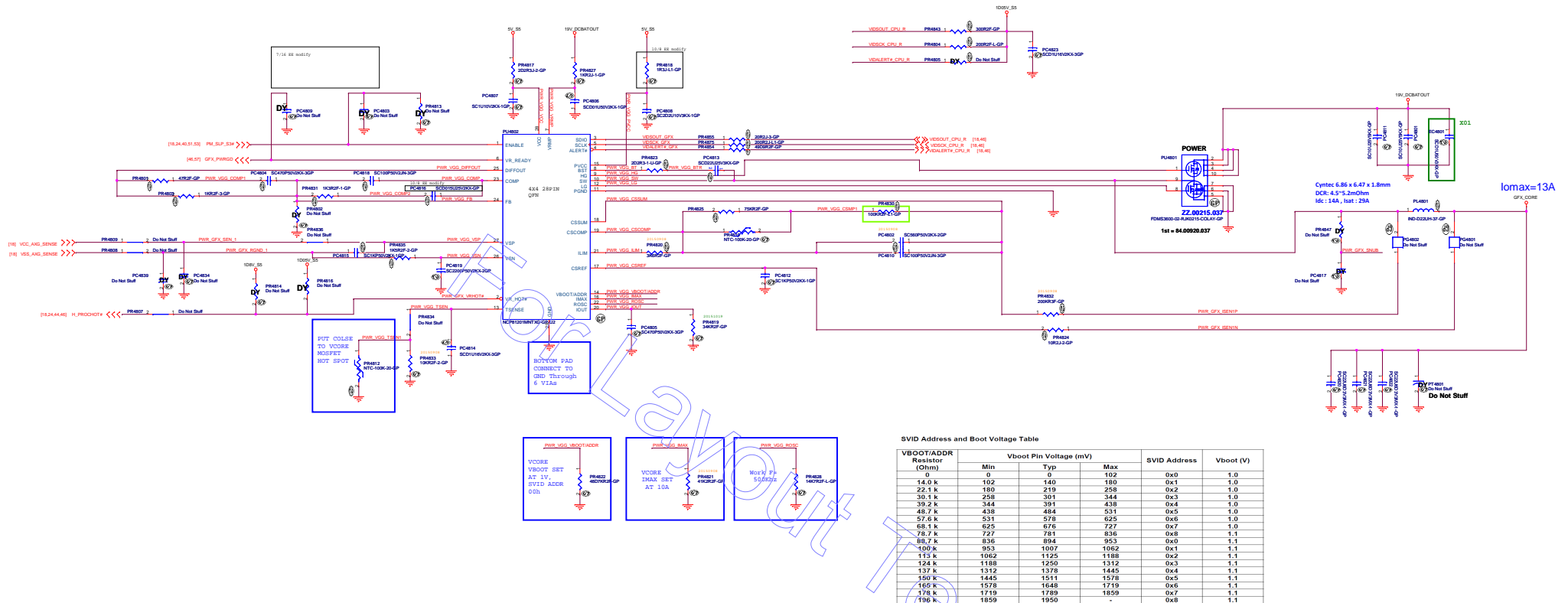
VBOOT/ADDR	SVID Address	Vboot (V)
Resistor (Ohm)		
0	0x0	1.0
14.0 k	0x1	1.0
22.1 k	0x2	1.0
30.1 k	0x3	1.0
39.2 k	0x4	1.0
48.7 k	0x5	1.0
57.6 k	0x6	1.0
67.8 k	0x7	1.0
78.7 k	0x8	1.1
88.7 k	0x0	1.1
100 k	0x1	1.1
113 k	0x2	1.1
124 k	0x3	1.1
137 k	0x4	1.1
150 k	0x5	1.1
165 k	0x6	1.1
178 k	0x7	1.1
196 k	0x8	1.1

SSID = CPU Regulator



Rocket BSW 1st

SSID = GFX Regulator



SVID/ADDR		Vboot Pin Voltage (mV)				SVID Address	Vboot (V)
Resistor (Ohm)		Min	Typ	Max			
0		0	0	102	0x0	1.0	1.0
14.0 k		102	140	180	0x1	1.0	1.0
22.1 k		180	219	258	0x2	1.0	1.0
30.1 k		258	301	344	0x3	1.0	1.0
39.2 k		344	391	438	0x4	1.0	1.0
48.7 k		438	484	531	0x5	1.0	1.0
57.6 k		531	578	625	0x6	1.0	1.0
68.1 k		625	676	727	0x7	1.0	1.0
78.7 k		727	781	836	0x8	1.1	1.1
89.7 k		836	894	953	0x9	1.1	1.1
100 k		953	1007	1062	0x10	1.1	1.1
113 k		1062	1125	1188	0x2	1.1	1.1
124 k		1188	1250	1312	0x3	1.1	1.1
137 k		1312	1378	1445	0x4	1.1	1.1
150 k		1445	1511	1578	0x5	1.1	1.1
165 k		1578	1648	1719	0x6	1.1	1.1
178 k		1719	1789	1859	0x7	1.1	1.1
190 k		1859	1930	2000	0x8	1.1	1.1



# Blanking

For Layout Team

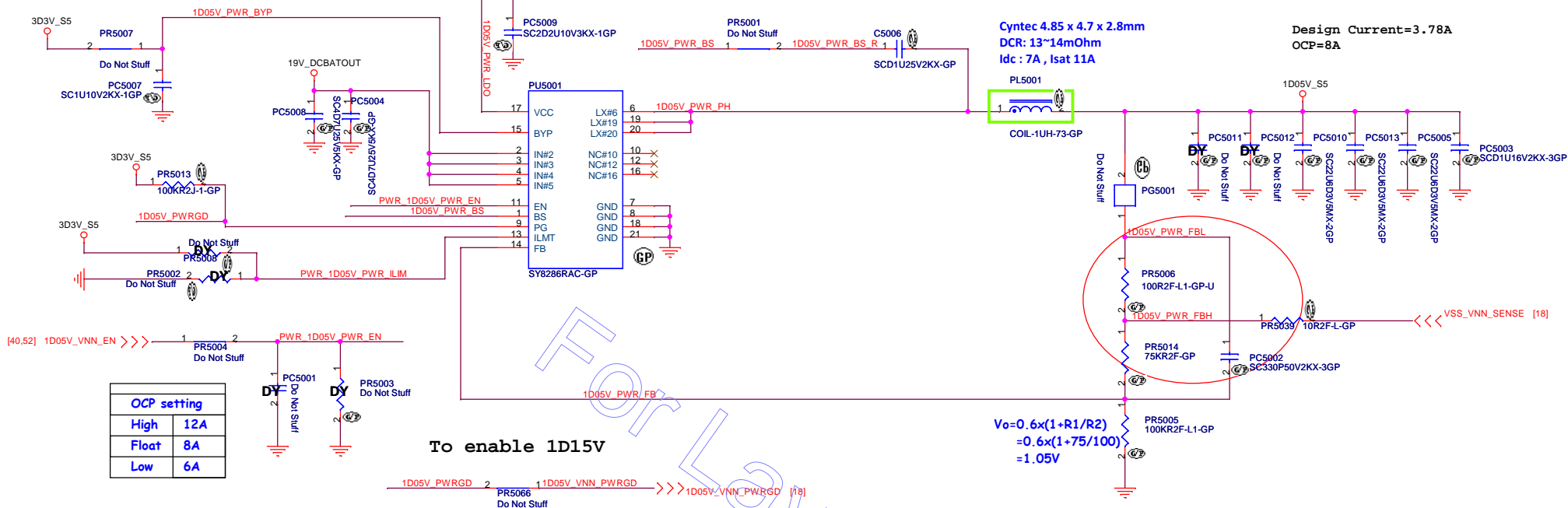
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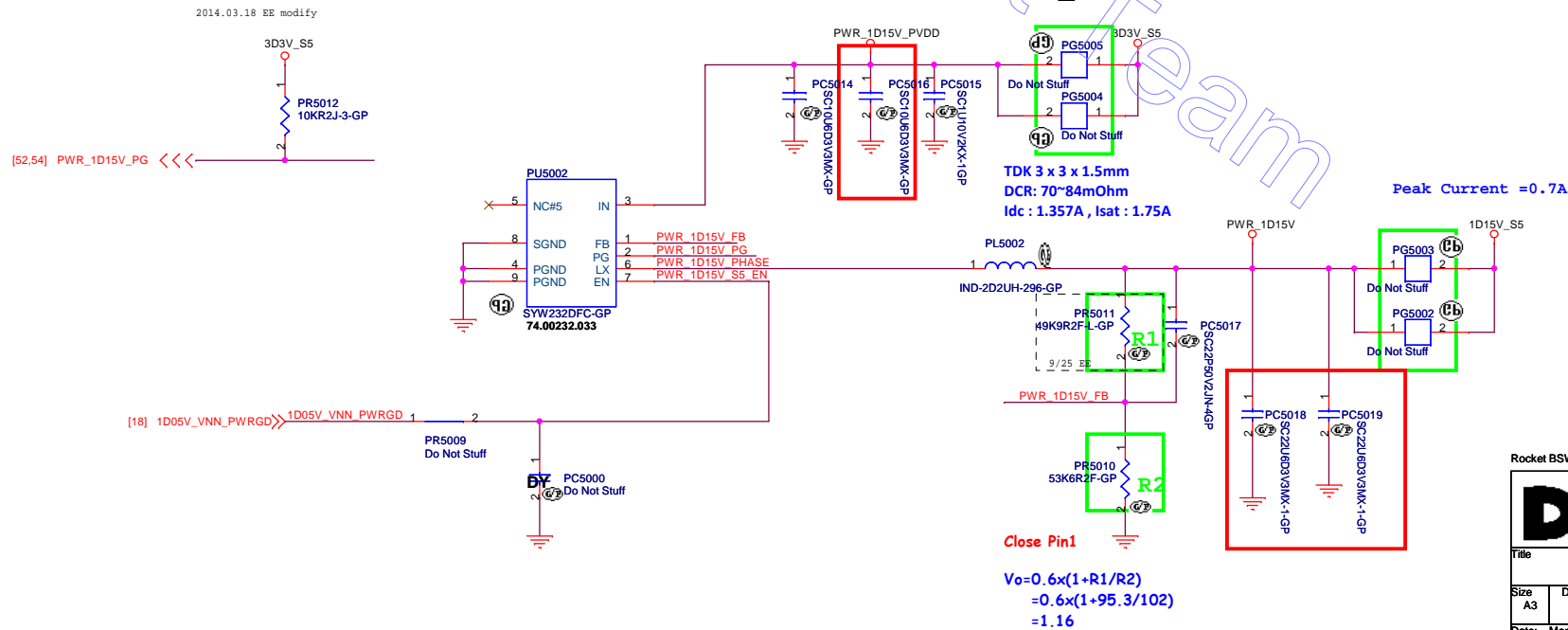
Title			<b>(Reserved)</b>		
Size	Document Number				Rev
A4	<b>Rocket BSW 11.6"</b>				<b>A00</b>
Date:	Monday, November 09, 2015			Sheet	49 of 109

## SY8286D for 1D05V



```
SSID = PWR.Plane.Regulator_1p8v
```

**SYW232 for 1D15V\_S5**



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Title

**DCDC VNN 1D05V 1D15V**Size  
A

Document Number

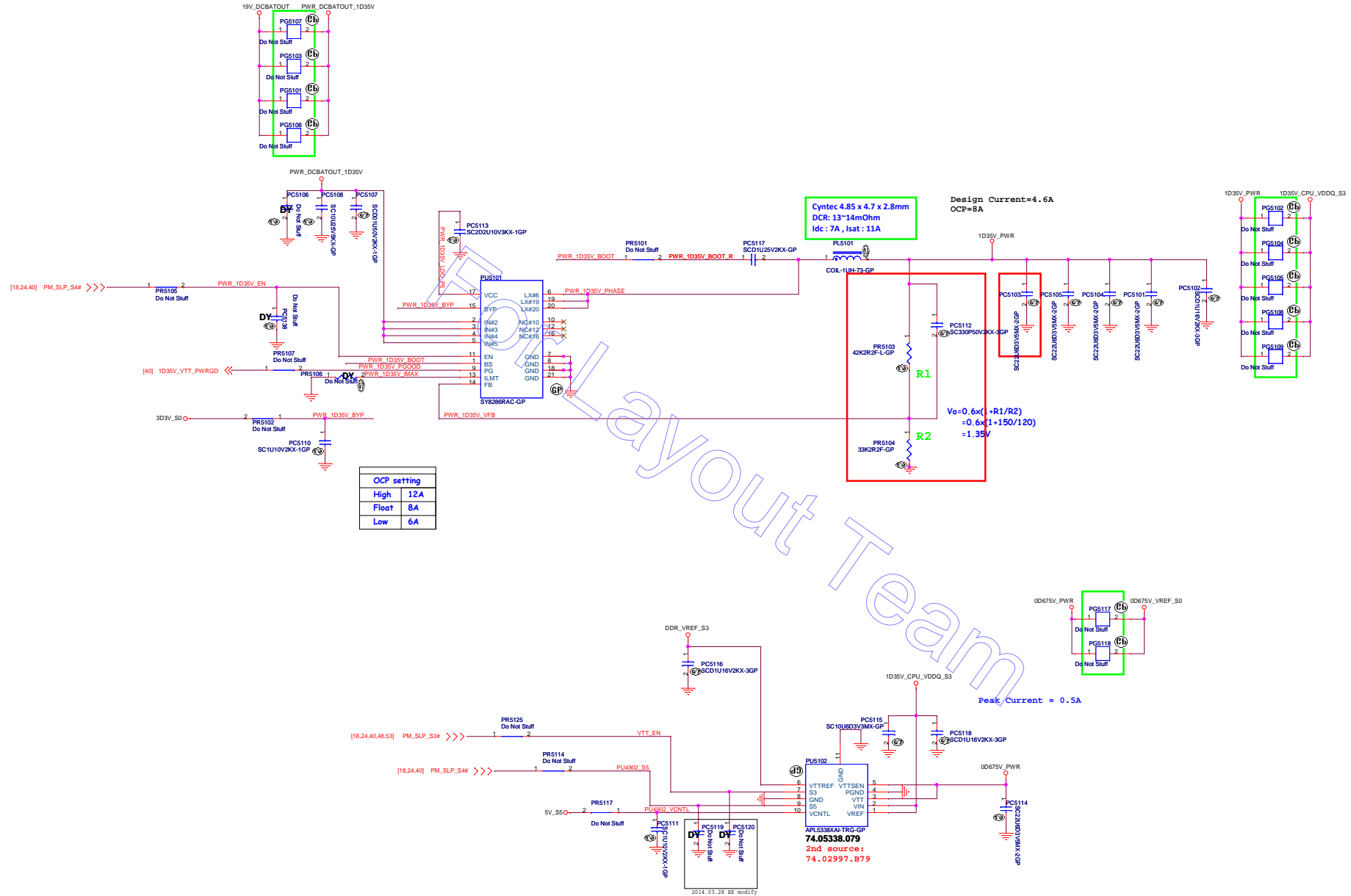
SIZE  
A

**Rocket BSW 11.6"**

Date: Monday, November 09, 2015

Sheet 50 of 109

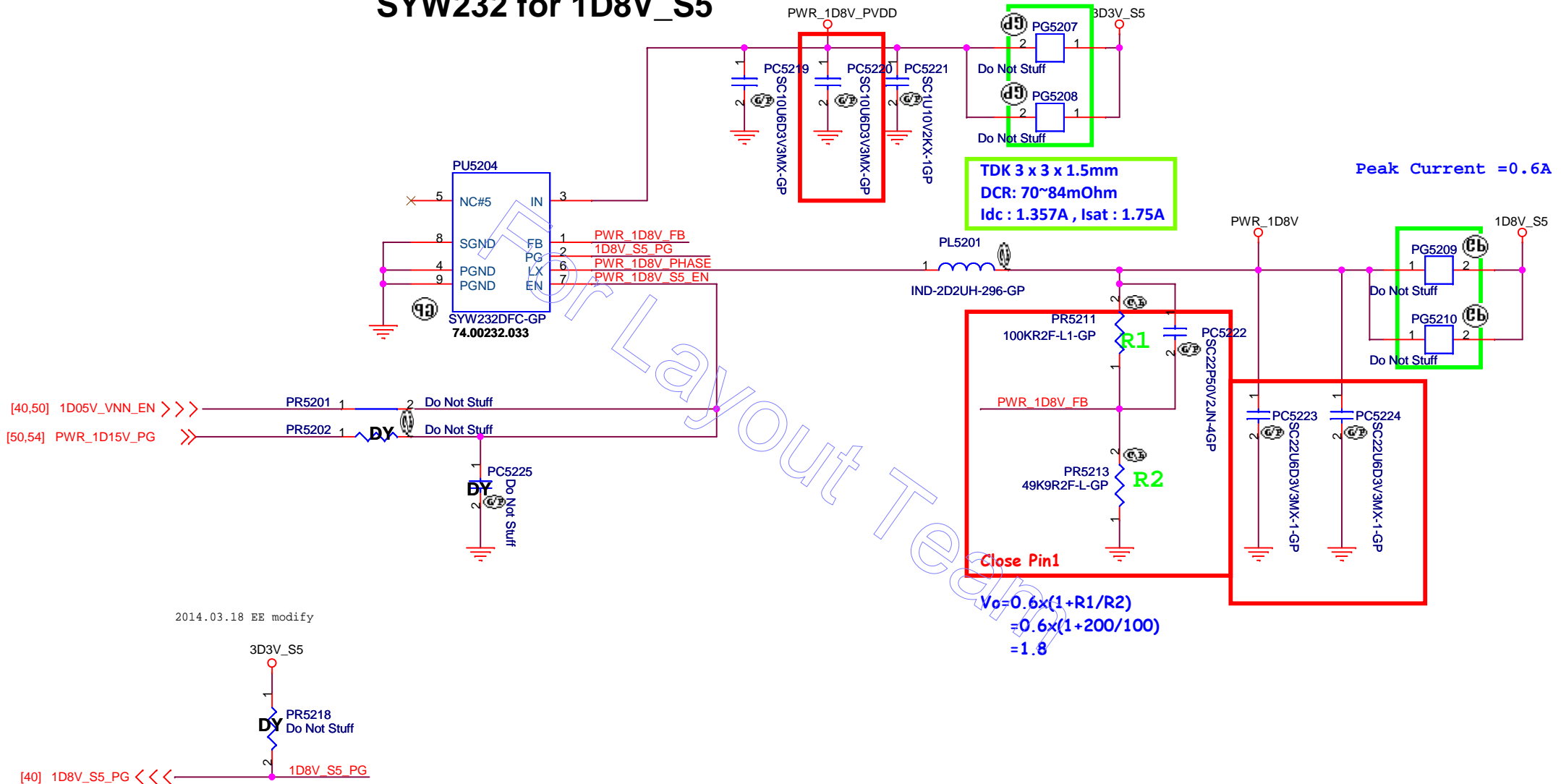
# SY8206D for 1D35V



Rocket BSW 1st

SSID = PWR.Plane.Regulator\_1p8v

## SYW232 for 1D8V\_S5



Rocket BSW 1st

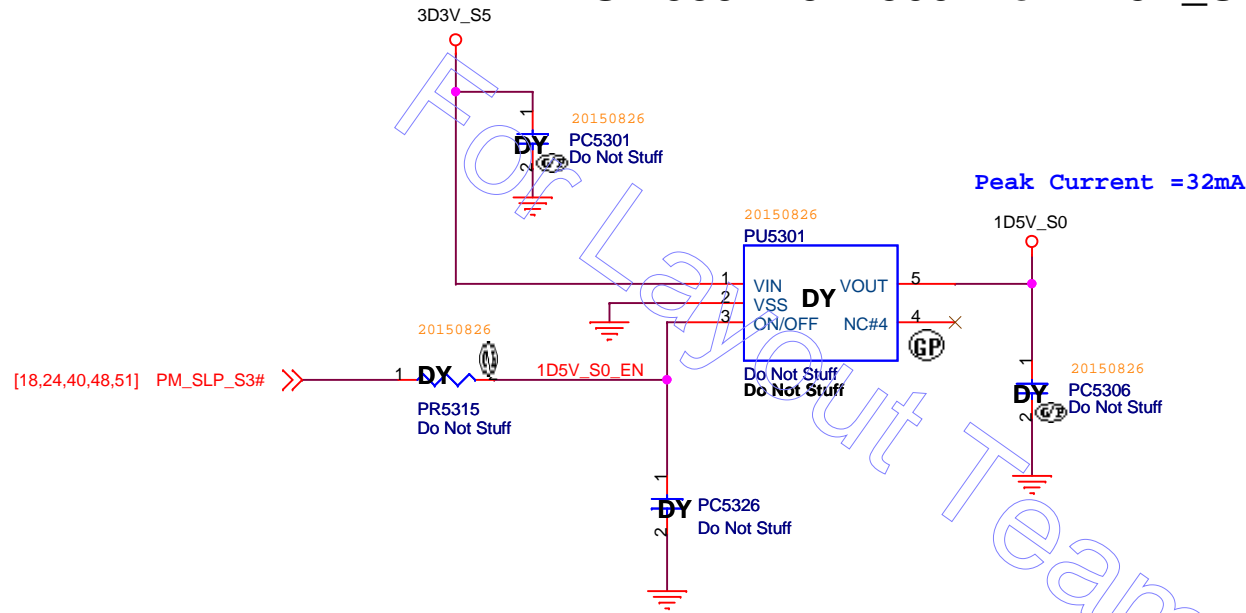


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Title					SYW232DFC_1D8V							
Size		Document Number				Rev						
A4		Rocket BSW 11.6"				A00						
Date:		Monday, November 09, 2015			Sheet		52		of		109	

## S-1339D15-M5001 for 1D5V\_S0



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**S1339D15 1D5V**

Size  
A4

Document Number

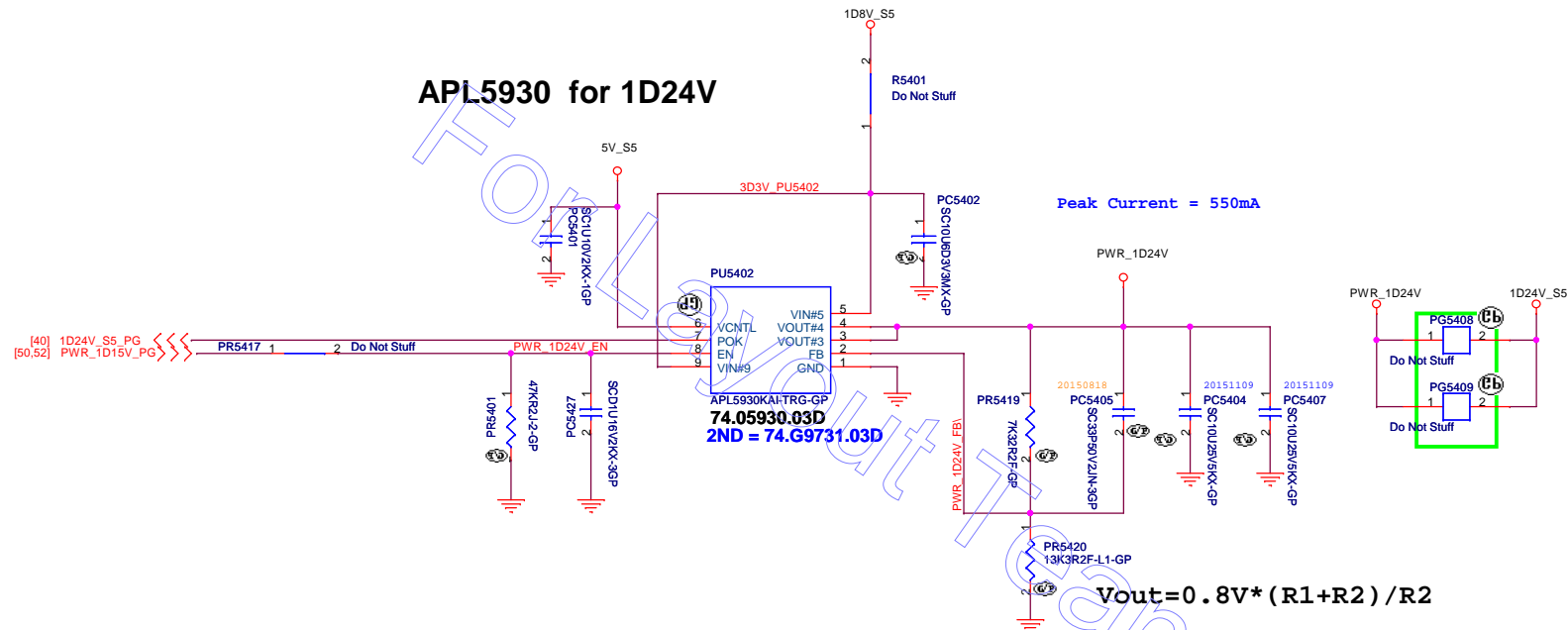
**Rocket BSW 11.6"**

Rev  
**A00**

Date: Monday, November 09, 2015

Sheet 53 of 109

# APL5930 for 1D24V



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Title

**APL5930\_1D24V**

Size  
A3

Document Number

**Rocket BSW 11.6"**

Rev

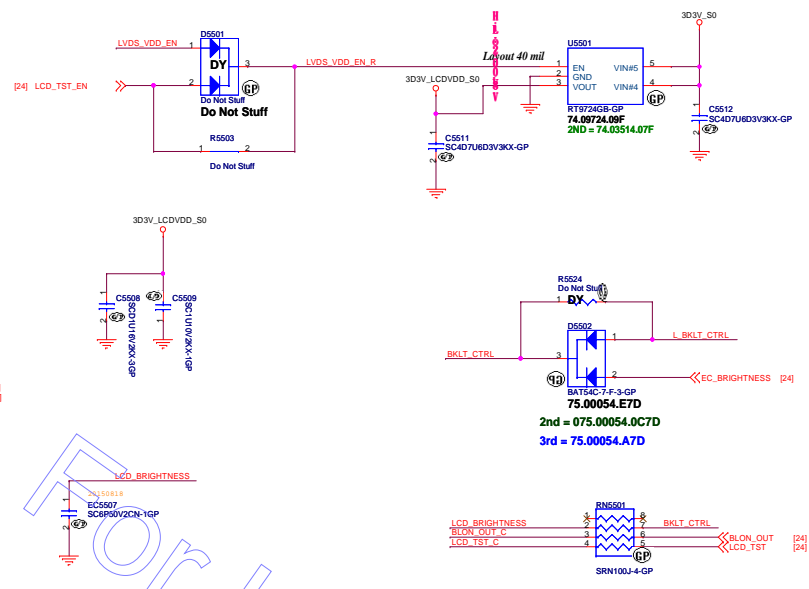
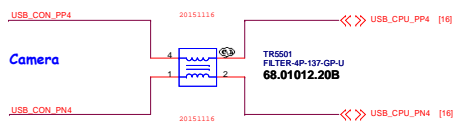
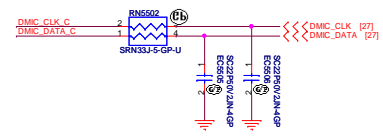
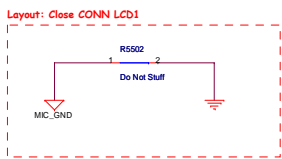
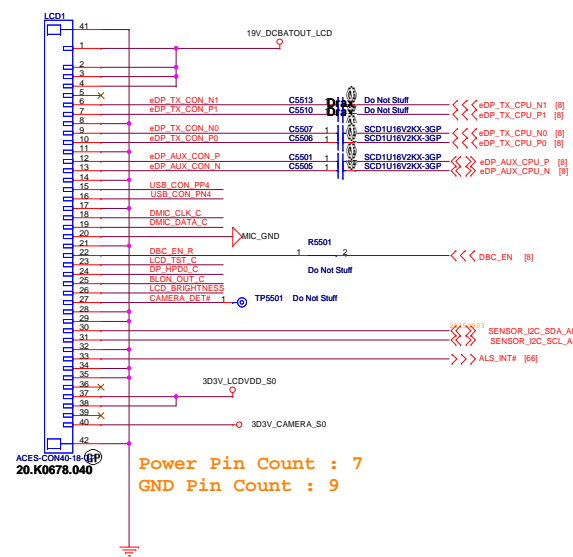
**A00**

Date: Monday, November 09, 2015

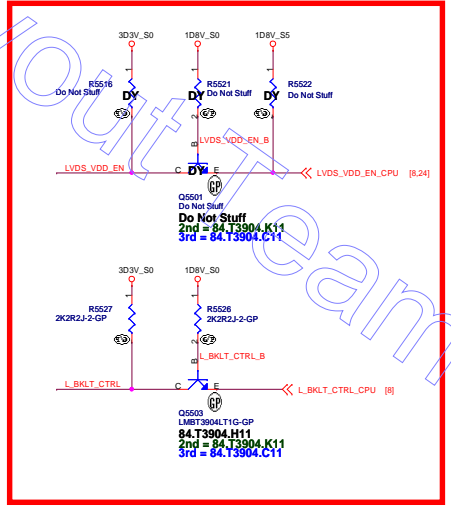
Sheet 54 of 109

SSID = VIDEO

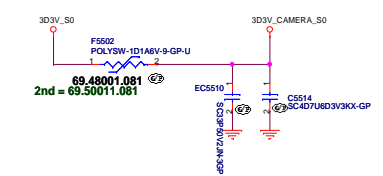
### Panel Conn.



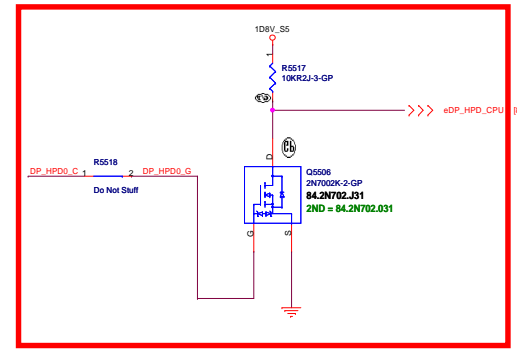
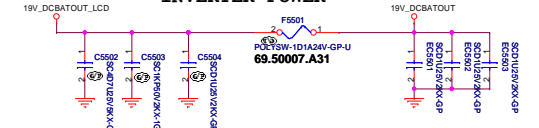
### Level shift



### CAMERA POWER




### INVERTER POWER



# Blanking

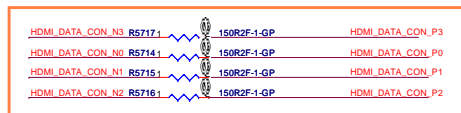
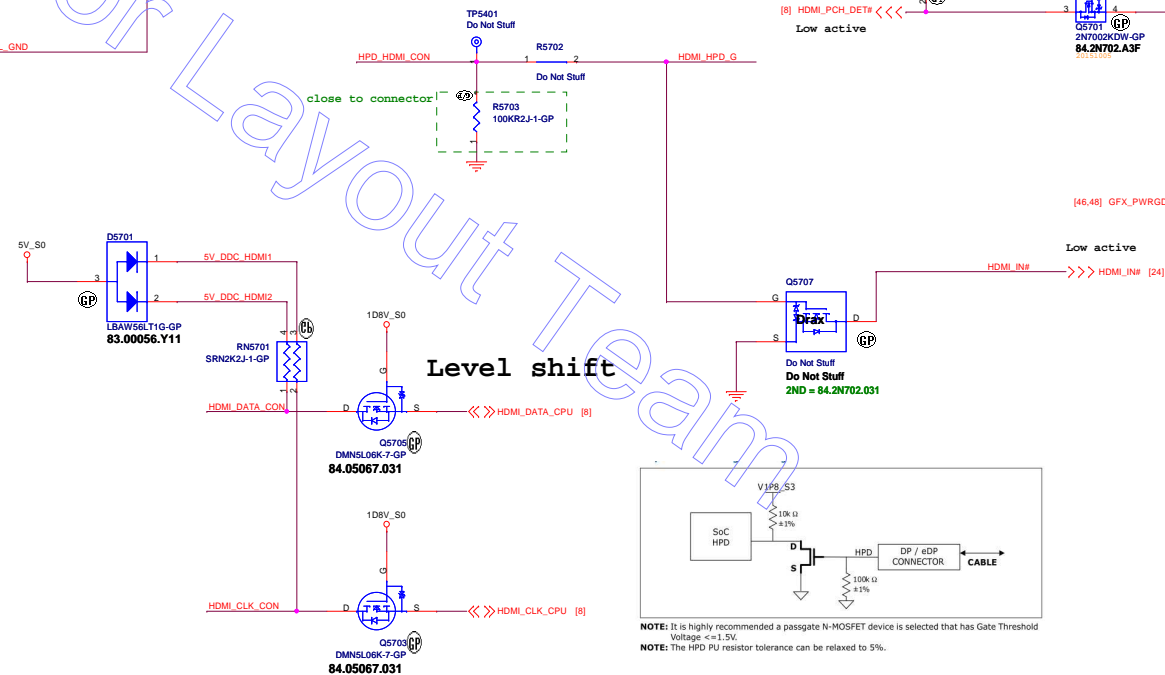
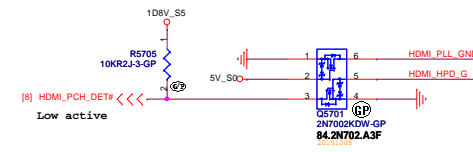
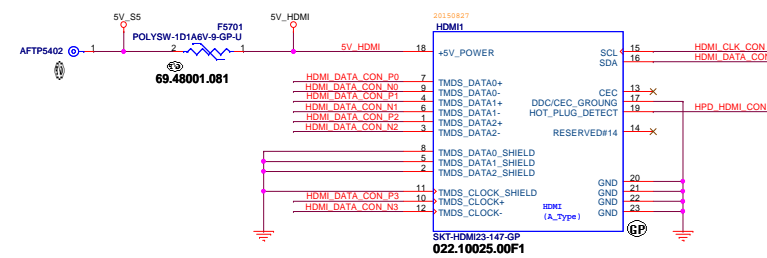
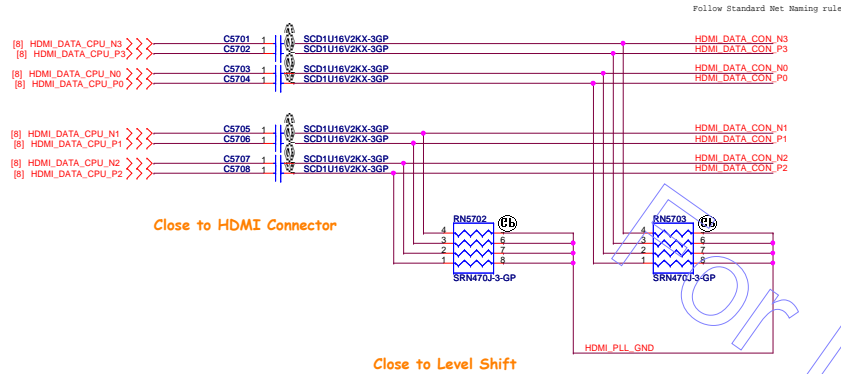
For Layout Team

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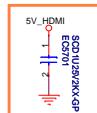
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Title			
<b>(Reserved)</b>			
Size A4	Document Number <b>Rocket BSW 11.6"</b>		Rev <b>A00</b>
Date: Monday, November 09, 2015		Sheet 56 of	109



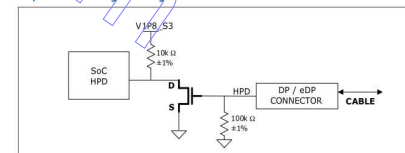
## HDMI Level Shifter & CONNECTOR



Reserve 150 ohm bridge resistance  
on the HDMI trace as circle for EMI



Reserve 0.1uF for ESD



**NOTE:** It is highly recommended a passgate N-MOSFET device is selected that has Gate Threshold Voltage  $\leq 1.5V$ .

**NOTE:** The HPD PU resistor tolerance can be relaxed to 5%.

#### 4.2.9 Hot Plug Detect Signal (HPD)

The ground reference for the Hot Plug Detect signal is the DDC/CEC Ground pin

Table 4-38 Required Output Characteristics of Hot Plug Detect Signal

Item	Value
High voltage level (Sink)	Minimum 2.4 Volts, Maximum 5.3 Volts
Low voltage level (Sink)	Minimum 0 Volts, Maximum 0.4 Volts
Output resistance	1000 ohms $\pm 20\%$

Table 4-39 Required Detection Levels for Hot Plug Detect Signal


Item	Value
High voltage level (Source)	Minimum 2.0 Volts, Maximum 5.3 Volts
Low voltage level (Source)	Minimum 0 Volts, Maximum 0.8 Volts

SSID = Display Port

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Title <b>(Reserved) Display Port</b>					
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Date: Monday, November 09, 2015			Sheet 58	of	109

SSID = DVI

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Title <b>(Reserved) DVI</b>			
Size	Document Number <b>Rocket BSW 11.6"</b>		Rev <b>A00</b>
Date: Monday, November 09, 2015		Sheet 59	of 109

SSID = SATA

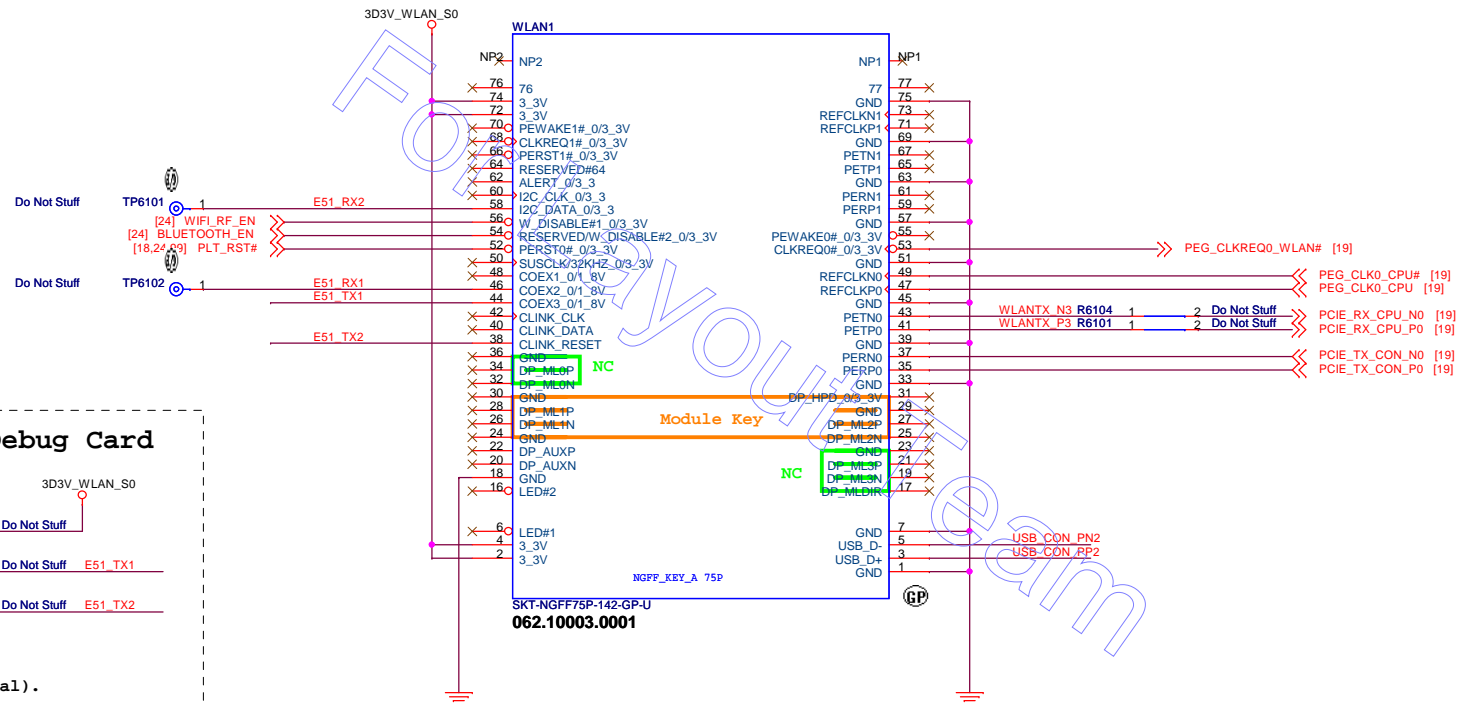
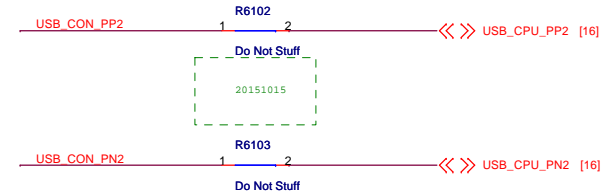
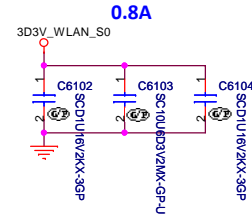
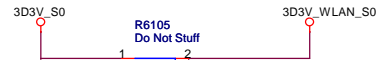
For Layout Team

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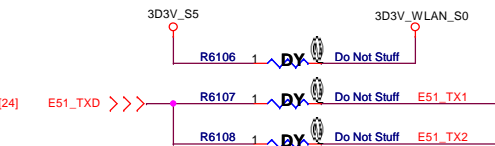
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Title			
<b>HDD</b>			
Size	Document Number		Rev
	<b>Rocket BSW 11.6"</b>		<b>A00</b>
Date: Monday, November 09, 2015		Sheet 60 of	109

SSID = WLAN

### *Mini Card Connector(802.11a/b/g)*



Reserved for NGFF Debug Card



EE Note:  
For NFGG Debug Card:  
Stuff R6106,R6107,R6108(optional).  
DY R6105

3D3V WLAN S0	1	AFTP6101
PEG CLKREQ0 WLAN#	1	AFTP6102
WIFI RF EN	1	AFTP6104
PLT_RST#	1	AFTP6105
BLUETOOTH_EN	1	AFTP6110
USB_CON PN2	1	AFTP6111
USB_CON PP2	1	AFTP6113

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Title

**WLAN**

Size

Document Number
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		<b>Rocket</b>
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### **Rocket BSW 11.6"**

Date: Monday, November 09, 2015

Sheet	61	of	109
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ev

SSID = WWAN

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Title

**(Reserved) WWAN**

Size

Document Number

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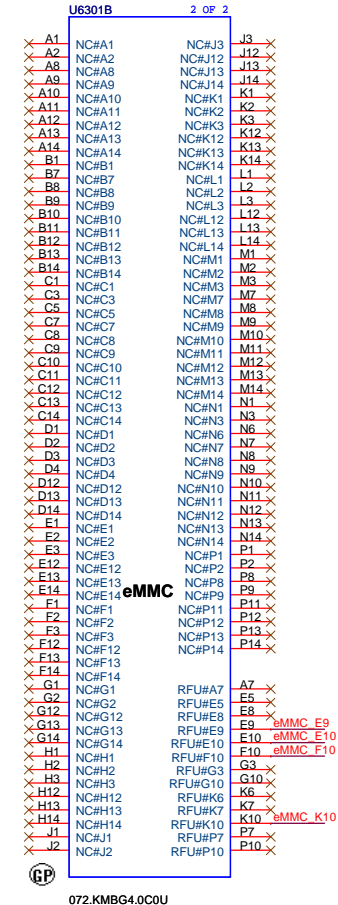
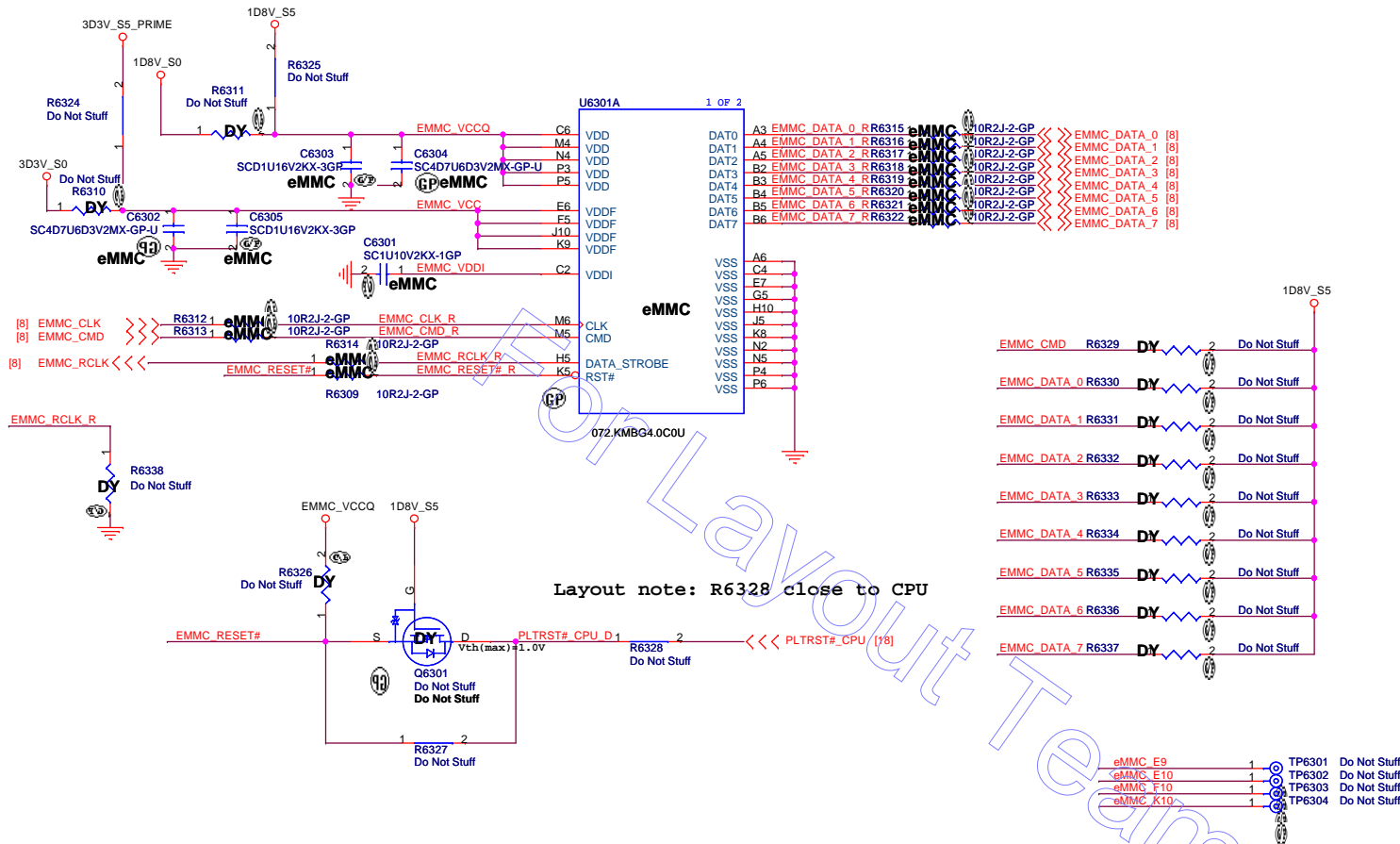
Rev

**A00**

Date: Monday, November 09, 2015

Sheet 62 of 109

# SSID = SSD-NGFF



	SKU1		SKU1-1		SKU2		SKU3	
CPU	BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4V	071.00BSW.0D0U	BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4V	071.00BSW.0D0U	BRASWELL 4c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4T	071.00BSW.0C0U	BRASWELL 4c FCBGA 1.6GHz 6W, GT 16EU, CELERON QS QJ4S	071.00BSW.0B0U
eMMC	Hynix/32G	J6PD1	Hynix/32G	J6PD1	SanDisk/32G	4P0NC	Samsung/32G	N8DV6
	SKU7		SKU8		SKU9			
CPU	BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4V	071.00BSW.0D0U	BRASWELL 2c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4V	071.00BSW.0D0U	BRASWELL 4c FCBGA 1.6GHz 6W, GT 12EU, CELERON QS QJ4T	071.00BSW.0C0U		
eMMC	Hynix/64G	WF56J	SanDisk/64G	7F7DJ	Samsung/64G	67D71		

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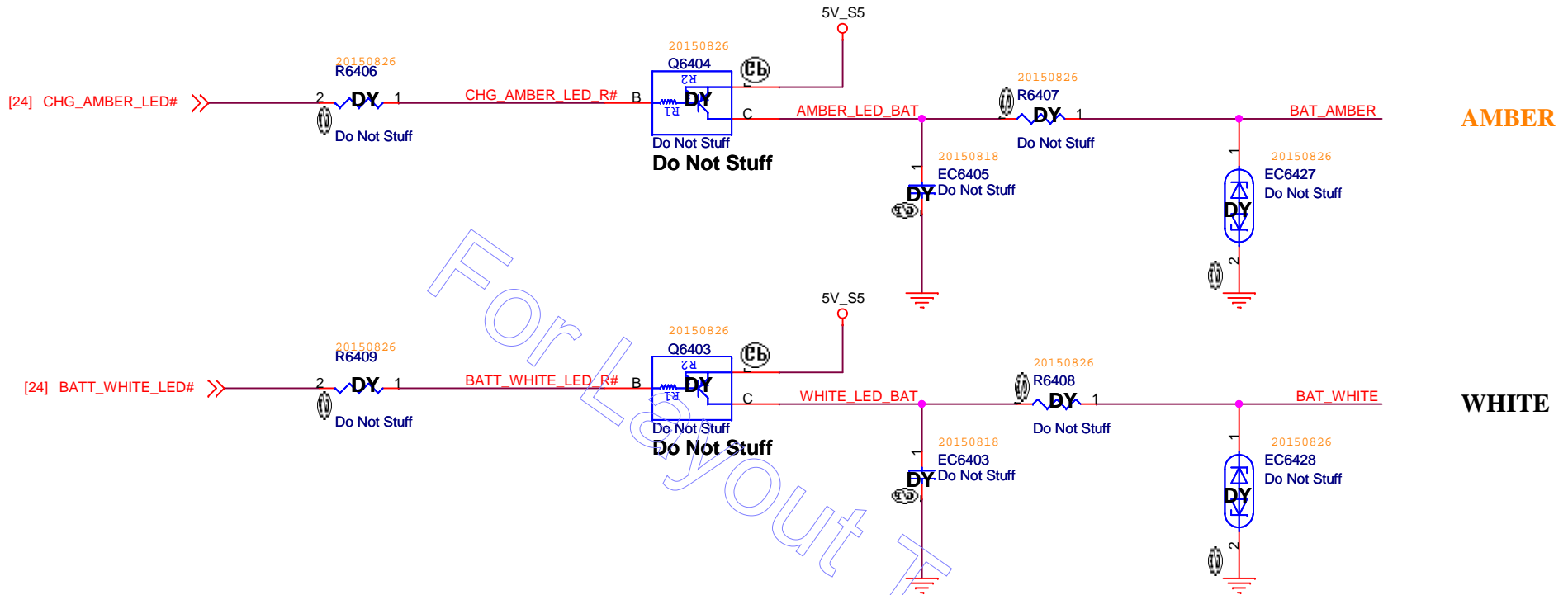
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Size: A3 Document Number: **Rocket BSW 11.6"** Rev: **A00**

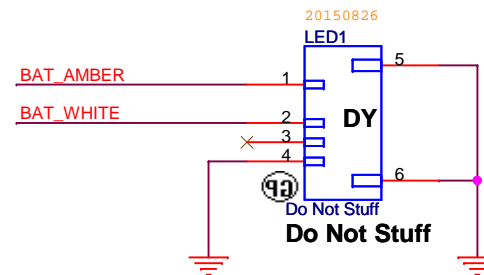
Date: Monday, November 09, 2015 Sheet: 63 of 109

SSID = LED / PWRBTN

Battery LED1 (AMBER\_LED)  
Low activated from KBC GPIO



Battery LED2 (WHITE\_LED)  
Low activated from KBC GPIO



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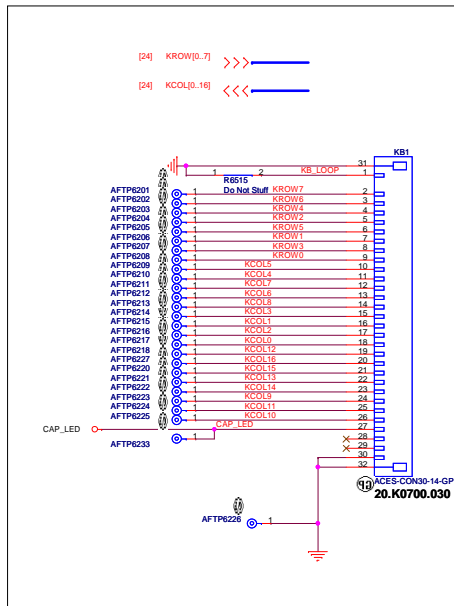
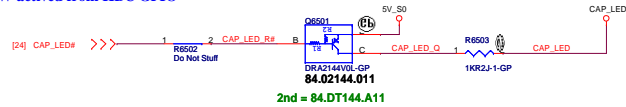
Title  
**LED / PWRBTN**

Size	Document Number	Rev
A4	<b>Rocket BSW 11.6"</b>	<b>A00</b>

Date: Monday, November 09, 2015 Sheet 64 of 109



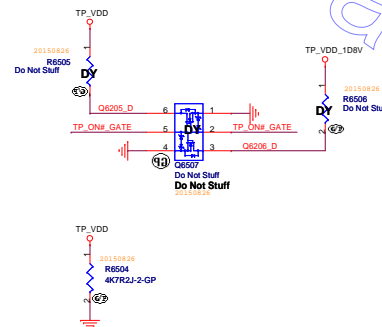
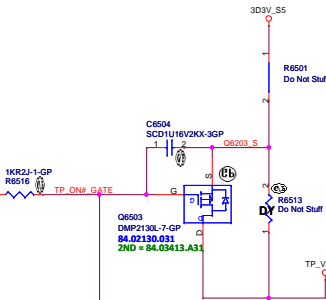
# CAP LED Control LOW active from KBC GPIO



CAP\_LED EC6506 1 Do Not Stuff

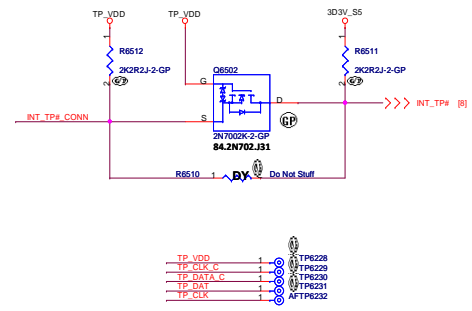
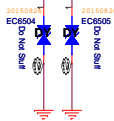
PIN#	SIGNAL
1	Diag_Loop=GPIO_1 (TPC)
2	KSI [7] = KBD S8
3	KSI [6] = KBD S7
4	KSI [4] = KBD S5
5	KSI [2] = KBD S3
6	KSI [5] = KBD S6
7	KSI [1] = KBD S2
8	KSI [3] = KBD S4
9	KSI [0] = KBD S1
10	KSO [5] = KBD D6
11	KSO [4] = KBD D5
12	KSO [7] = KBD D8
13	KSO [6] = KBD D7
14	KSO [8] = KBD D9
15	KSO [3] = KBD D4
16	KSO [1] = KBD D2
17	KSO [2] = KBD D3
18	KSO [0] = KBD D1
19	KSO [12] = KBD D13
20	KSO [16] = KBD D17
21	KSO [15] = KBD D16
22	KSO [13] = KBD D14
23	KSO [14] = KBD D15
24	KSO [9] = KBD D10
25	KSO [11] = KBD D12
26	KSO [10] = KBD D11
27	CopsLock LED
28	N/C
29	N/C
30	GND

TP\_ON# >>> 1



TP\_OC\_DATA <<< 16

TP\_OC\_CLK <<< 16



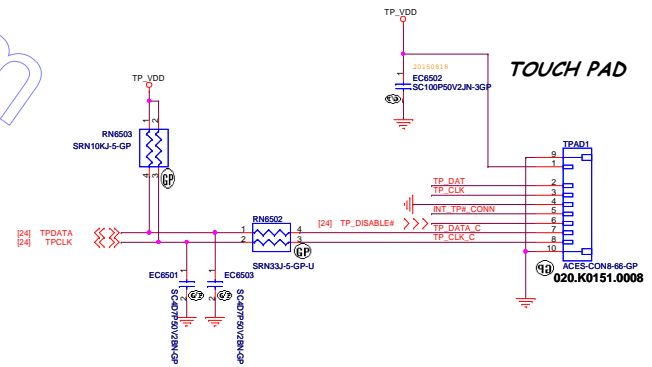
TP\_VDD

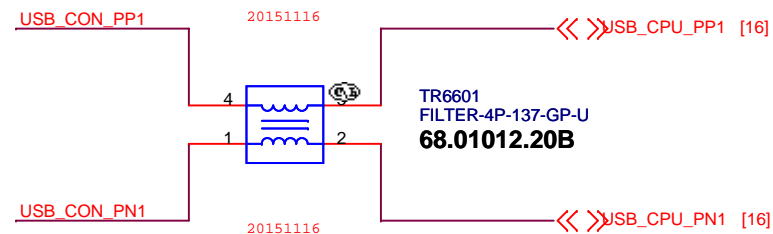
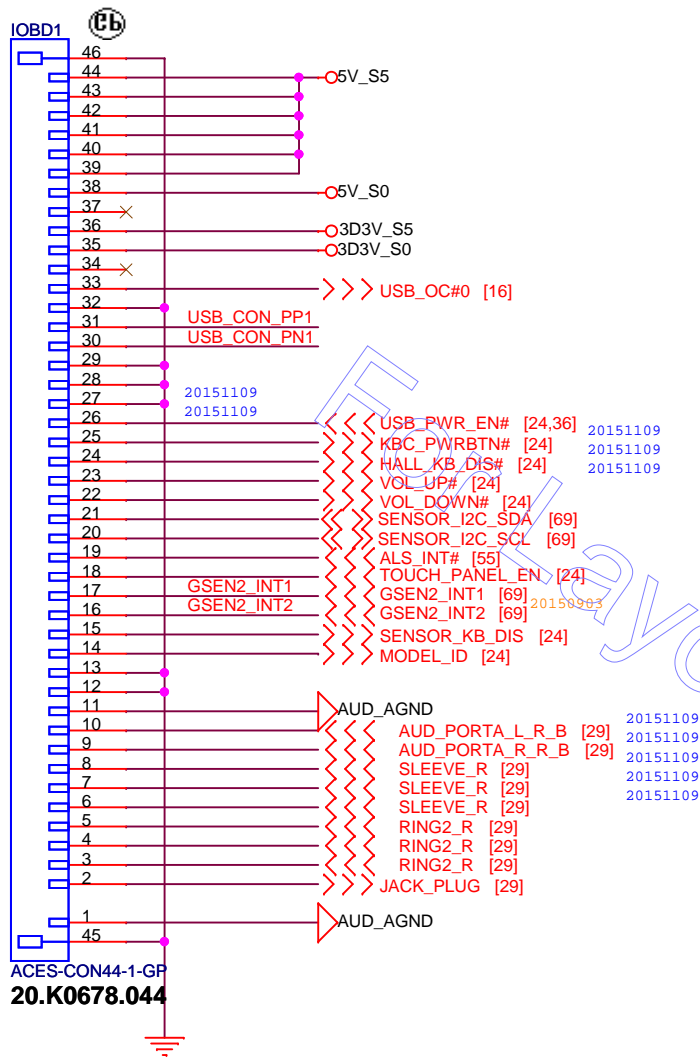
TP\_CLK\_C

TP\_DATA\_C

TP\_DAT

TP\_CLK





Power Pin Count : 10  
GND Pin Count : 5

USB3.0 Port2

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Title

**IO Board CONN**

Size

Document Number

Rev

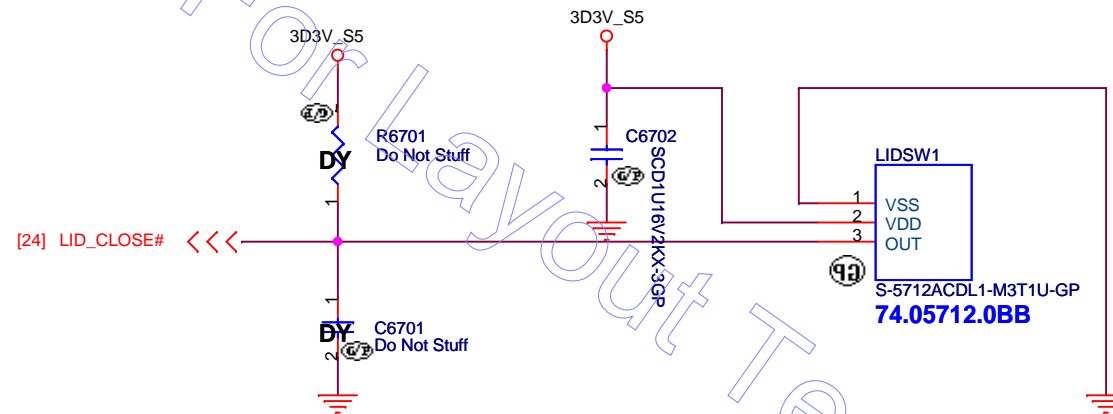
A4

**Rocket BSW 11.6"**

**A00**

Date: Monday, November 16, 2015

Sheet 66 of 109



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Title

**Hall Sensor**

Size  
A4

Document Number

**Rocket BSW 11.6"**

Rev  
**A00**

Date: Monday, November 09, 2015

Sheet 67 of 109

SSID = Debug CONN

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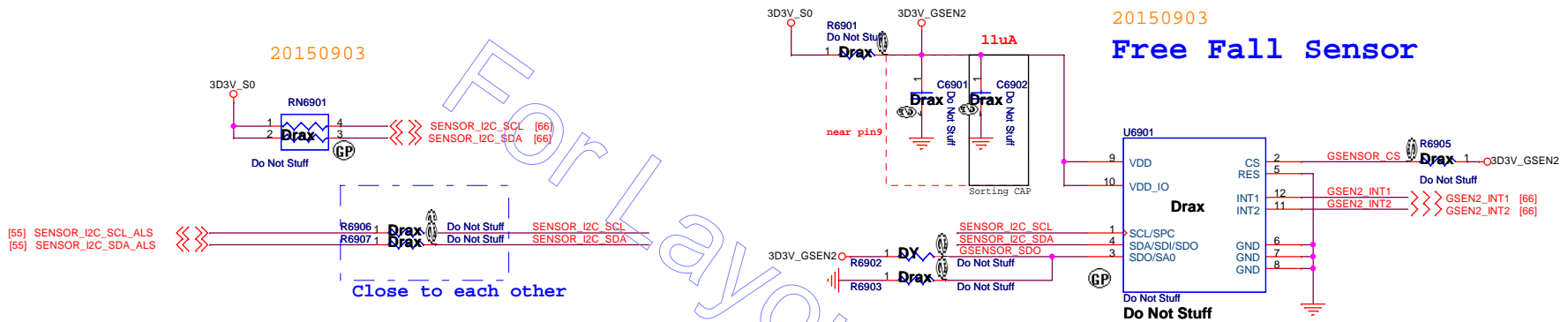
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Title			<b>(Reserved) Debug CONN</b>		
Size	Document Number				Rev
A4	<b>Rocket BSW 11.6"</b>				<b>A00</b>
Date: Monday, November 09, 2015			Sheet	68	of 109

SSID = Sensor




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Title			
Sensor			
Size A3	Document Number		Rev
	Rocket BSW 11.6"		A00
Date: Monday, November 09, 2015		Sheet 69 of	109

SSID = Free Fall Sensor

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Title <b>Free Fall Sensor</b>			
Size A4	Document Number <b>Rocket BSW 11.6"</b>		Rev <b>A00</b>
Date: Monday, November 09, 2015		Sheet 70	of 109

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Title **(Reserved)Thunderbolt (1/5)**

Size A4	Document Number <b>Rocket BSW 11.6"</b>	Rev <b>A00</b>
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Date: Monday, November 09, 2015 Sheet 71 of 109

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Date: Monday, November 09, 2015 Sheet 72 of 109



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Title **(Reserved)Thunderbolt (3/5)**

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------------	--	-------------------

Date: Monday, November 09, 2015 Sheet 73 of 109

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Title **(Reserved)Thunderbolt (4/5)**

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------------	--	-------------------

Date: Monday, November 09, 2015 Sheet 74 of 109

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Title **(Reserved)Thunderbolt (5/5)**

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Date: Monday, November 09, 2015 Sheet 75 of 109

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Title **(Reserved)GPU (1/5) PEG**

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Title **(Reserved)GPU (2/5) DIGITAL**

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Date: Monday, November 09, 2015 Sheet 77 of 109

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Title **(Reserved)GPU (3/5) VRAM**

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Date: Monday, November 09, 2015 Sheet 78 of 109

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Title **(Reserved)GPU (4/5) GPIO**

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------------	--	-------------------

Date: Monday, November 09, 2015 Sheet 79 of 109

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Date: Monday, November 09, 2015 Sheet 80 of 109



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Title **(Reserved)VRAM1,2 (1/4)**

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Date: Monday, November 09, 2015 Sheet 81 of 109

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Title **(Reserved)VRAM3,4 (2/4)**

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Date: Monday, November 09, 2015 Sheet 82 of 109

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Title **(Reserved)VRAM5,6 (3/4)**

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Date: Monday, November 09, 2015 Sheet 83 of 109

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Title **(Reserved)VRAM7,8 (4/4)**

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Title **(Reserved)VGA\_CORE**

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Date: Monday, November 09, 2015 Sheet 85 of 109

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Rocket BSW 1st



**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

**(Reserved)DISCRETE VGAPOWER**

Size

Document Number

Rev

**Rocket BSW 11.6"**

**A00**

Date: Monday, November 09, 2015

Sheet 86 of 109

# Blanking

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A4

Document Number

**Rocket BSW 11.6"**

Rev  
**A00**

Date: Monday, November 09, 2015

Sheet 87 of 109

# Blanking

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Title  
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Size A4	Document Number <b>Rocket BSW 11.6"</b>	Rev <b>A00</b>
------------	--	-------------------

Date: Monday, November 09, 2015 Sheet 88 of 109



20150828  
**34.4YW18.001**  
SPRING-171-GP  
SPR1



20150827  
**34.4YW18.001**  
SPRING-171-GP  
SPR2



20150827  
**34.4YW18.001**  
SPRING-171-GP  
SPR3



20151008  
**34.34S02.002**  
SPRING-98-GP  
SPR4



20151008  
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SPRING-98-GP  
SPR5

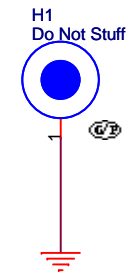


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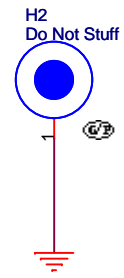


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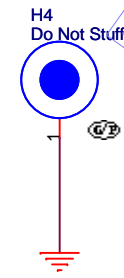
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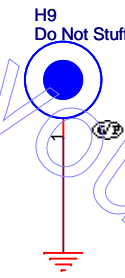
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**Do Not Stuff**

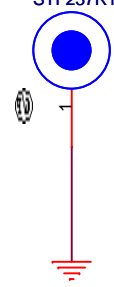


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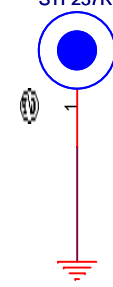


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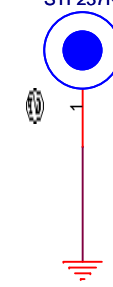
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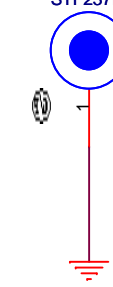
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HS2  
STF237R117H67-3-GP




**34.4OX45.101**  
HS3  
STF237R117H67-3-GP



**34.4OX45.101**  
HS4  
STF237R117H67-3-GP



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Title <b>UNUSED PARTS/EMI Capacitors</b>		
Size A4	Document Number <b>Rocket BSW 11.6"</b>	Rev <b>A00</b>
Date: Monday, November 09, 2015		Sheet 89 of 109

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Title **(Reserved)NFC Connector**

Size A4	Document Number <b>Rocket BSW 11.6"</b>	Rev <b>A00</b>
------------	--	-------------------

Date: Monday, November 09, 2015 Sheet 90 of 109

# Blanking

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Title  
**(Reserved) TPM**

Size A4	Document Number <b>Rocket BSW 11.6"</b>	Rev <b>A00</b>
------------	--	-------------------

Date: Monday, November 09, 2015 Sheet 91 of 109

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Title **(Reserved)Finger Print**

Size A4	Document Number <b>Rocket BSW 11.6"</b>	Rev <b>A00</b>
------------	--	-------------------

Date: Monday, November 09, 2015 Sheet 92 of 109

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Title

(Reserved)Express Card

Size  
A3

Document Number  
**Rocket BSW 11.6"**

Date: Monday, November 09, 2015

Rev  
**A00**

Sheet 93 of 109

D

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Title			
<b><i>(Reserved)Smart Card Socket</i></b>			
Size A4	Document Number <b><i>Rocket BSW 11.6"</i></b>		Rev <b><i>A00</i></b>
Date:	Monday, November 09, 2015	Sheet 94 of	109

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Title

**(Reserved)SW GFX eDP**

Size  
A4

Document Number

**Rocket BSW 11.6"**

Rev  
**A00**

Date: Monday, November 09, 2015

Sheet 95 of 109

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Title

***(Reserved)Bottom Docking***

Size  
A4

Document Number

***Rocket BSW 11.6"***

Rev  
***A00***

Date: Monday, November 09, 2015

Sheet 96 of 109



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Title **(Reserved)LAN**

Size A4	Document Number <b>Rocket BSW 11.6"</b>	Rev <b>A00</b>
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Date: Monday, November 09, 2015 Sheet 97 of 109

# Blanking

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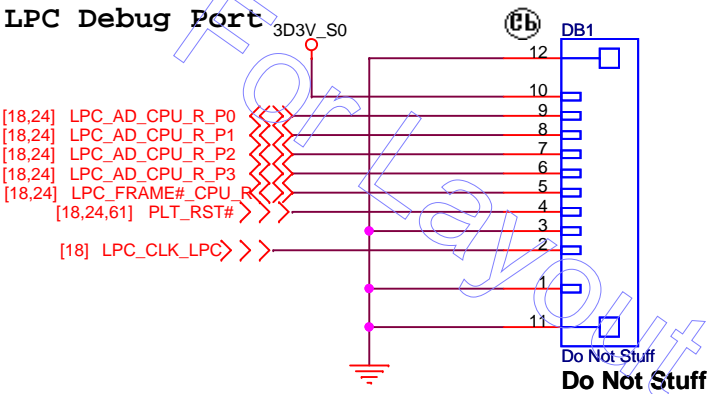


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Title **(Reserved)LAN SWITCH**


Size	Document Number	Rev
	<b>Rocket BSW 11.6"</b>	<b>A00</b>

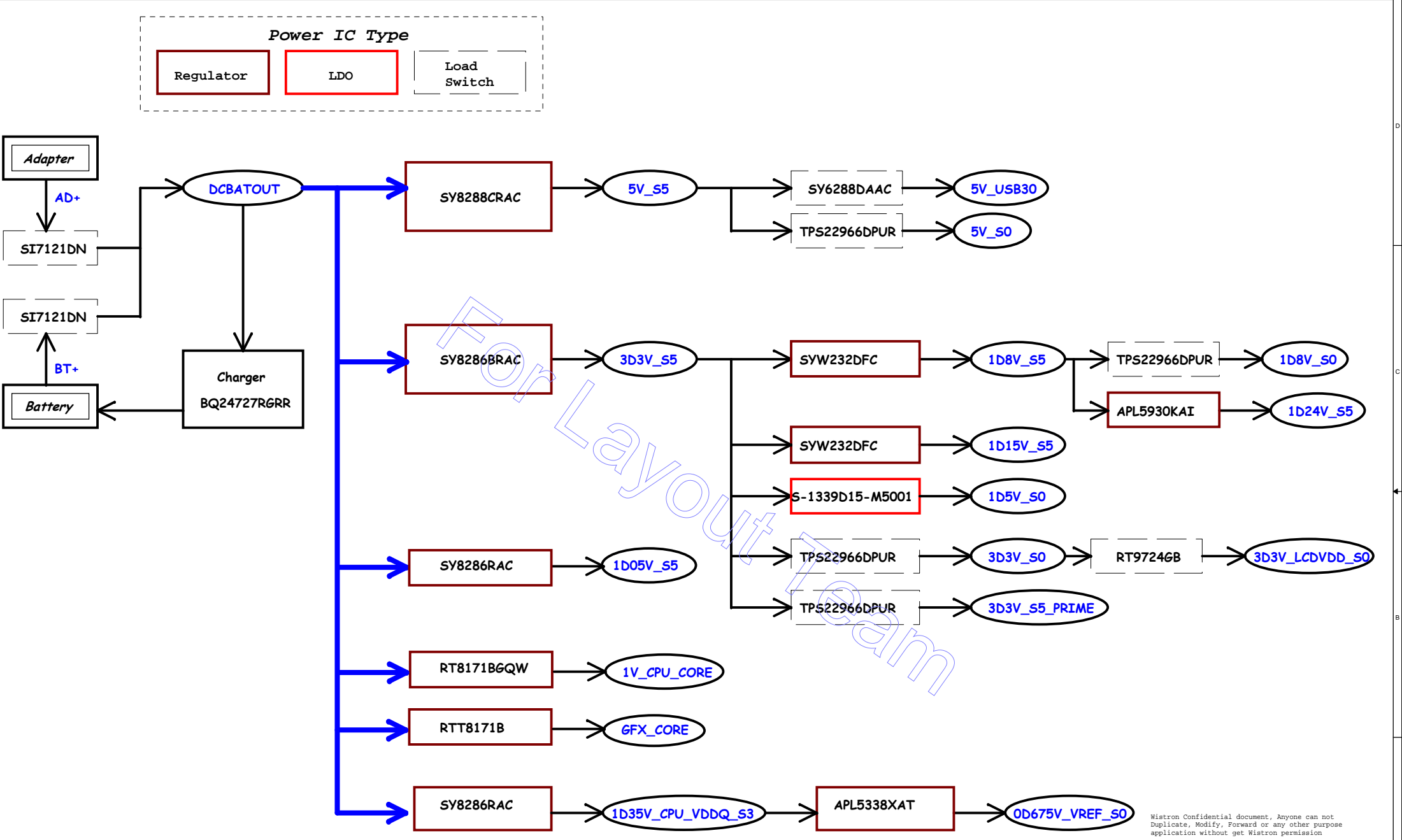
SSID = DEBUG PORT



20.F1180.010: Dummy Pad with solder mask is ZZ.00PAD.GV1

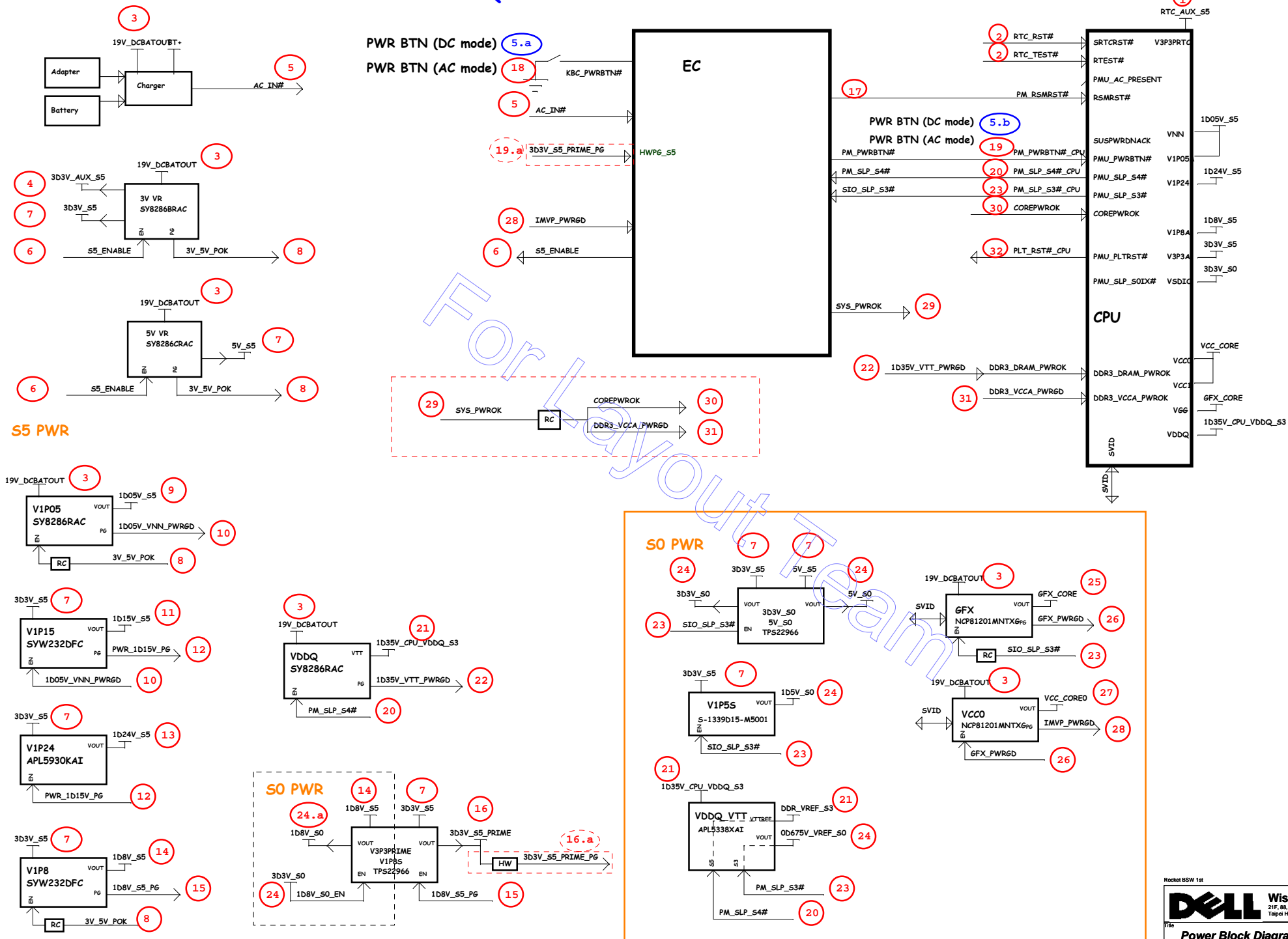
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Title			
<b>CPU XDP</b>			
Size A4	Document Number		Rev <b>A00</b>
Date: Monday, November 16, 2015		Sheet 99 of	109



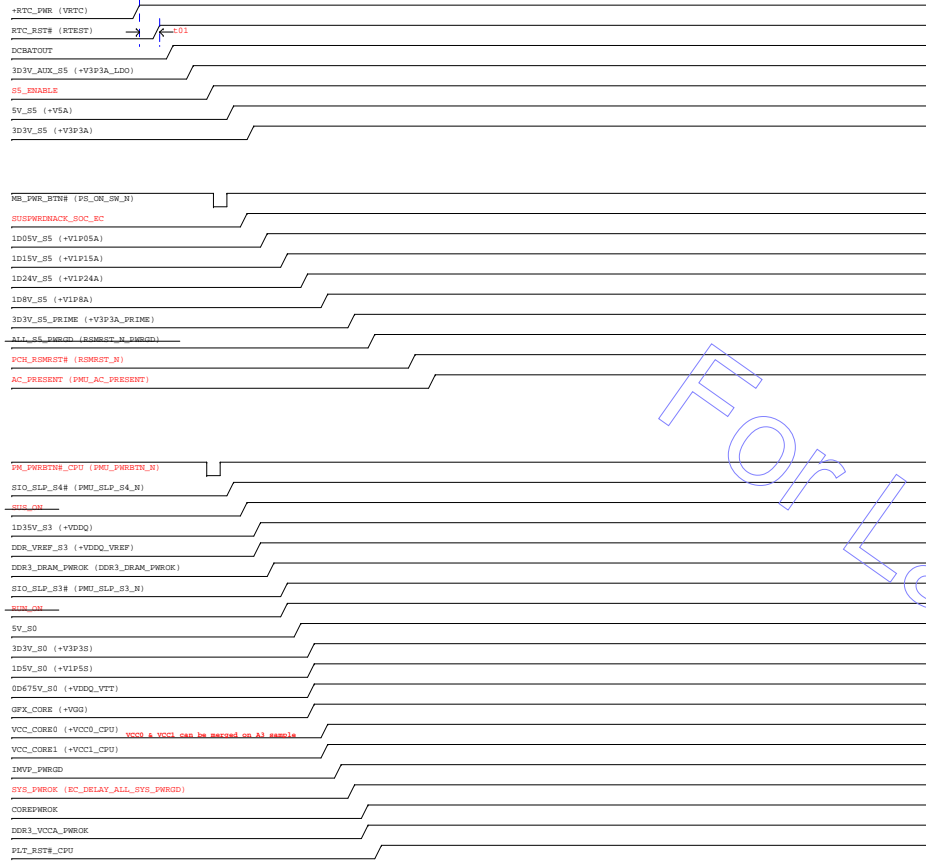
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## Braswell POWER UP SEQUENCE DIAGRAM



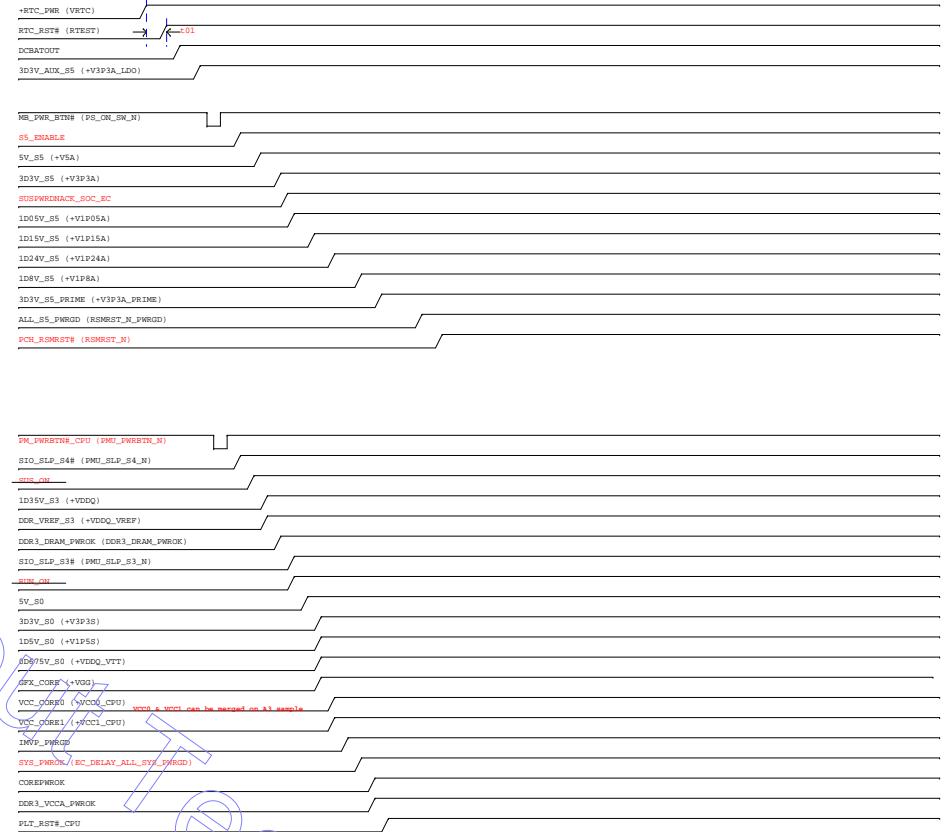
# Intel-Power Up Sequence

(AC mode) Red word : RBC GP20



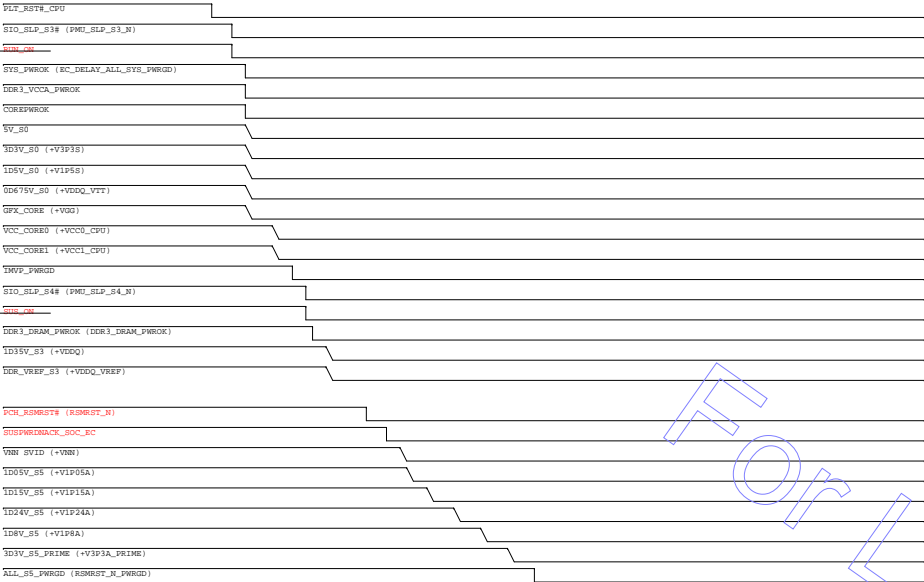
# Intel-Power Up Sequence

(DC mode) Red word : RBC GP20



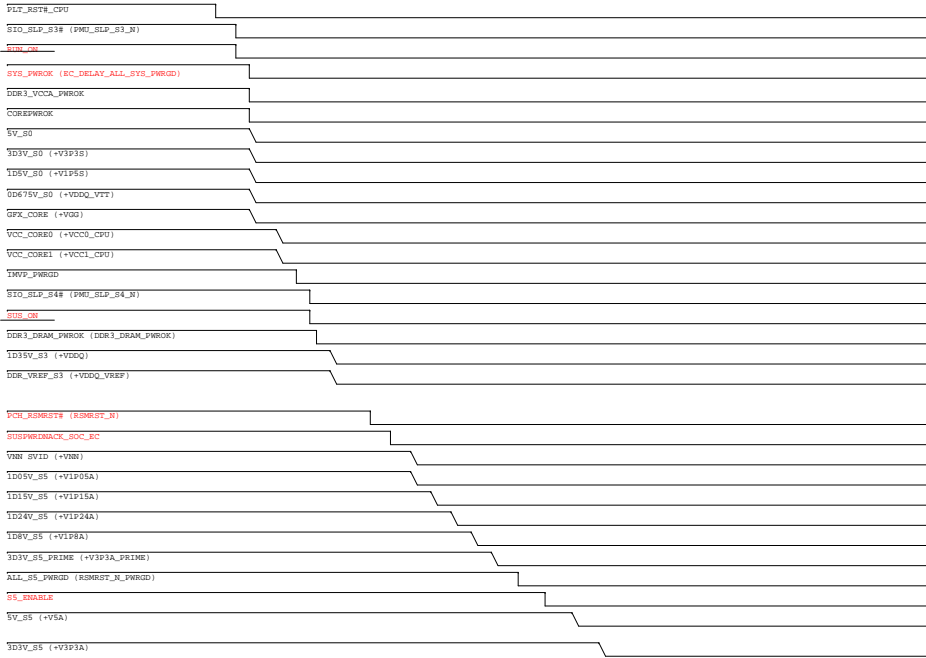
Intel-Power Down Sequence

(AC mode) Red word : X8C GP10



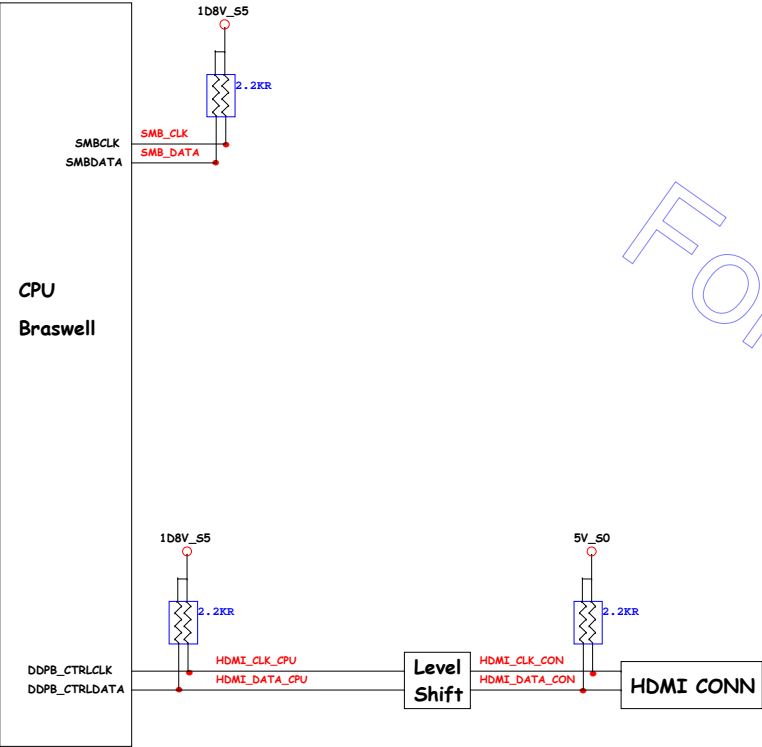
Intel-Power Down Sequence

(DC mode) Red word : X8C GP10

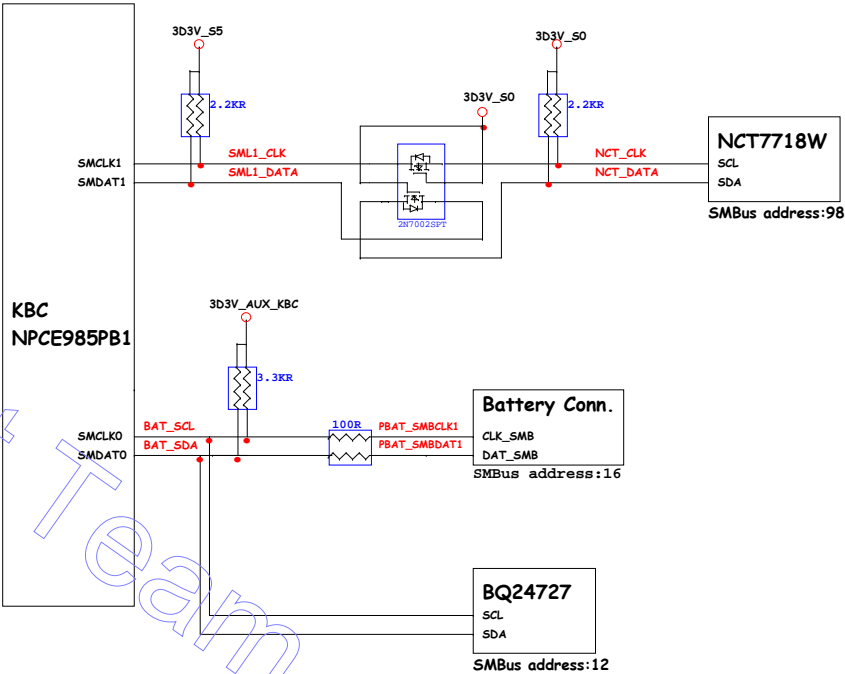


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PCH SMBus Block Diagram

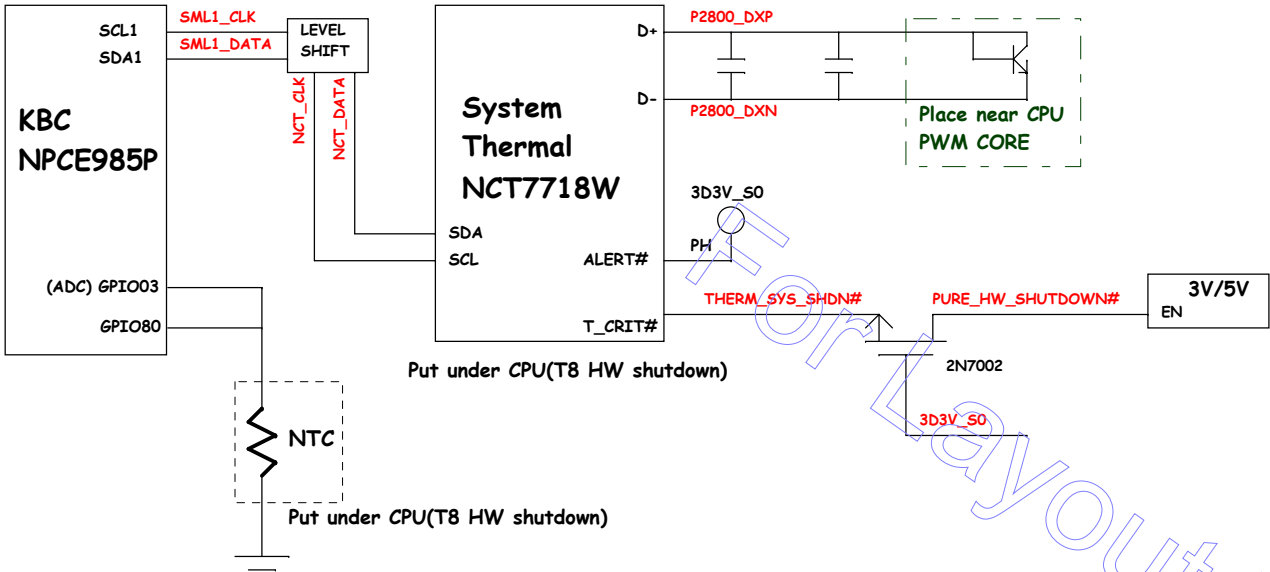


KBC SMBus Block Diagram

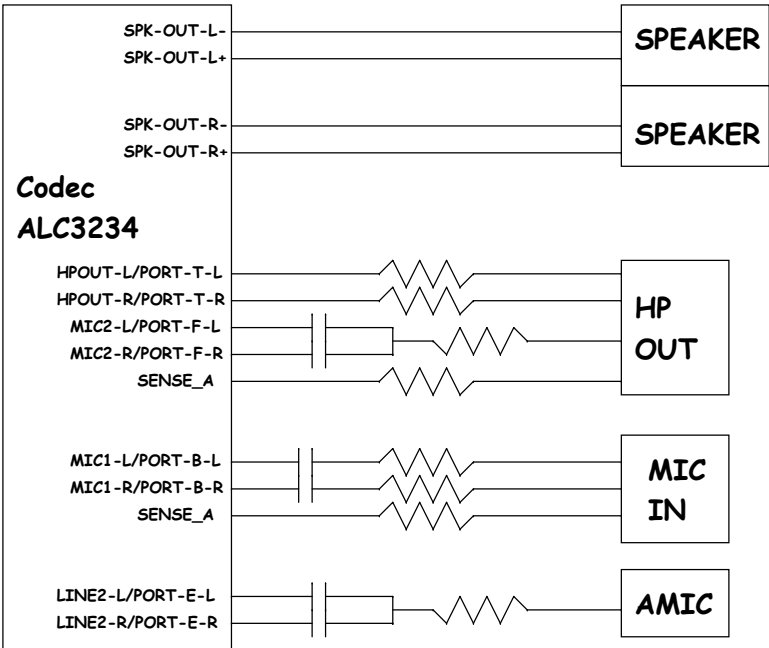




# Thermal Block Diagram



# Audio Block Diagram

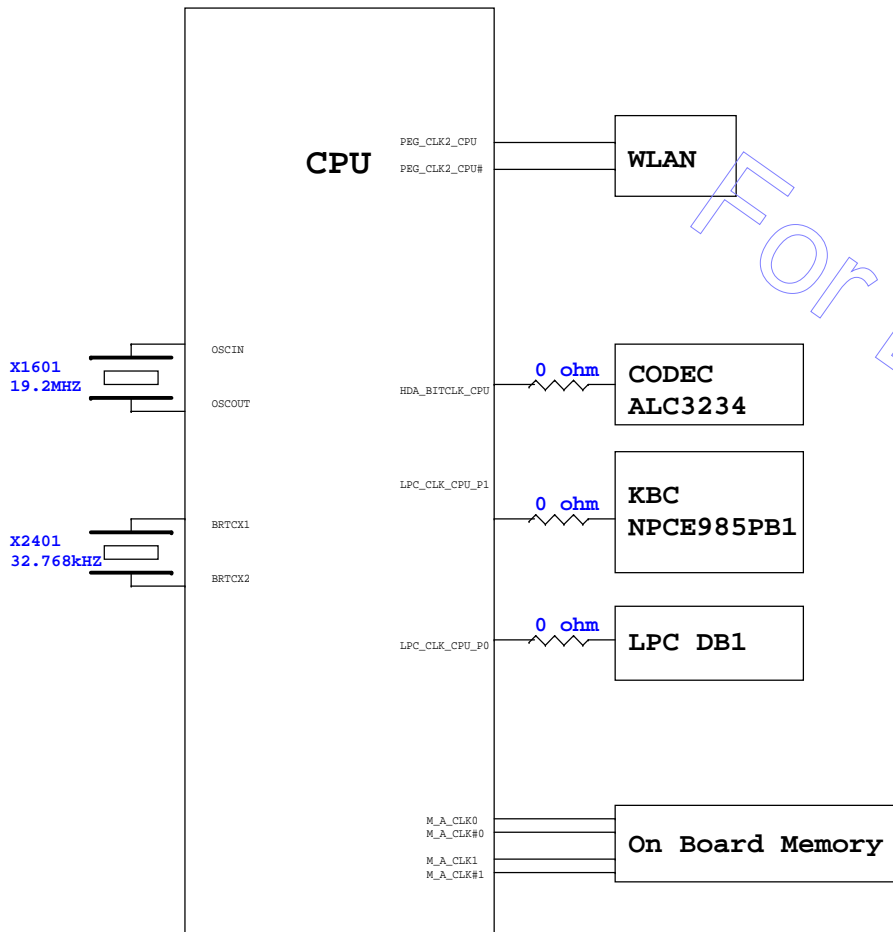


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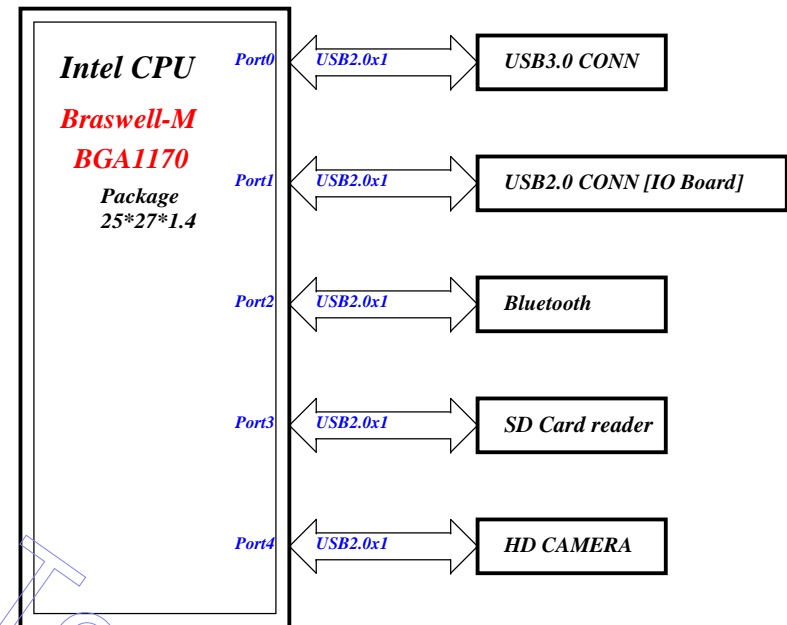


Title		Thermal/Audio Block Diagram	
Size	Document Number	Rev	A00
Date: Monday, November 09, 2015		Sheet	105 of 109

## CLK Block Diagram



## USB2.0 Port Block Diagram



Rocket BSW 1st

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						
12						
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SizeDocument Number

Rocket BSW 11.6"

RevA00

DateMonday, November 09, 2015Sheet107of109

Item	Page#	Date	Request By	Issue description			Solution Description			Rev.					
				For Layout Team											

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